INSTRUCTION MANUAL

MODEL 200

AVERAGE AND PEAK RESPONDING LIMITER

May 1973



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SECTION 1.0 GENERAL INFORMATION

The Inovonics 200 is a dual-function unit which incorporates both fast-acting peak limiting and average-responding automatic gain control circuits. Features, several of which are unique to the Model 200, include:

Calibrated, detented attenuators for independent control of INPUT GAIN, PEAK CEILING, and AVERAGE LEVEL LIMIT. This type of control offers the ability to preset (or reset) these adjustments to given values.

A SLOW A.G.C. mode which may be employed to minimize long-term variations in program level.

An exclusive PEAK HOLD feature that can sample the level of musical selections during an initial preview play-through, and automatically set a proper dubbing level for subsequent master transfer.

Low distortion (even at low frequencies) assured by unique open-loop gain control and ripple-cancelling circuitry.

Instant display of limiting action by peakresponding indicators. An optional remote-mounting Gain Reduction Meter may be located at the console.

1.1 SPECIFICATIONS

Frequency Response:

 ± 0.5 dB 20Hz - 20kHz

Signal-to-Noise Ratio:

Greater than 75dB, referred to +4dBm line level

<u>Distortion</u> (THD @ +4dBm line level with 15dB Limiting or Average Level Reduction):

	50Hz - 200Hz	200Hz - 20kHz
Peak Limiter NORM Release: FAST Release:	0.5% max. 0.8% max.	0.3% max. 0.4% max.
Average Level Limiter:	0.4% max.	0.3% max.
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Limiters OFF:

0.15% max., 20Hz - 20kHz @ +23dBm

Limiter Timing:

Peak Limiter

NORM Attack: less than lus/dB-limiting
DELAYED Attack: 2ms fixed delay + 0.5ms/dB-limiting
NORM Release: approx. 30ms/dB-limiting
FAST Release: approx. 6ms/dB-limiting
PEAK HOLD Attack: less than 10us/dB-limiting
PEAK HOLD Release (drift): less than 0.1dB/minute

Average Level Limiter

NORM Attack and Release: approx. 50ms/dB-limiting SLOW A.G.C.: Operates in conjunction with NORM mode and requires approx. 10 seconds for complete gain reduction or restoration.

Stereo Coupling: Two or more units may be interconnected for ganged gain reduction.

Input:

Sensitivity: Adjusts in 2dB steps to accommodate input levels between -10 and +10VU.

Impedance: 100K, unbalanced (transformer optional)

Output: Line output feeds 600 ohm line or bridging input at +4 or +8dBm. Clipping level +24dBm.

Panel Controls: (SEE 3.1)

Panel Indicators: Peak-responding indicators display gain state of Limiter circuit: LINEAR (no limiting); AVG. GAIN REDUCTION; PEAK LIMIT.

Power Requirement: 105 - 130VAC, 50 / 60Hz, 10 watts Size and Weight: 1-3/4" X 19" X 6-1/2", 71bs.

Accessories:

Remote-mounting Gain Reduction Meter
Input isolation transformer

1.1.1 As terminology relating to Audio Limiters is not standardized, and as some operating parameters are difficult to specify in universally nunderstood terms, Inovonics welcomes the opportunity to answer any questions which may arise from the specifications as stated. Such correspondence should be addressed to the Engineering Department of Inovonics, at the address appearing on the front of this manual.

SECTION 2.0 INSTALLATION

- 2.1 Upon receipt of the equipment, inspect for shipping damage. If any such damage is found, notify the carrier at once; if not, proceed as outlined below. Save the original shipping carton and materials for future shipment.
- 2.2 The Model 200 Average and Peak Responding Limiter is packaged to mount in a standard 19-inch rack, requiring only 1-3/4 inches of rack space per channel.
- 2.3 A screw-terminal barrier strip provides connections for input, output, and optional remote-mounting Gain Reduction Meter. An additional jack permits interconnecting two or more units for ganged gain reduction.
- 2.4 As shipped, the Model 200 is calibrated for a +4dBm line. Should operation with a +8dBm line be required, see Section 4.0 for recalibration procedures.
- 2.5 No line termination switch is provided or necessary, as the very low source impedance obviates any shift in characteristics, whether or not the output is terminated in 600 ohms. Should the equipment which feeds the Model 200 require output loading, an external 600 ohm resistor may be placed across the input terminals; otherwise, the input impedance is a nominal "Hi-Z bridging".

3.1 OPERATION

3.1.1 The operating controls for both the Average Level Limiter and Peak Limiter are respectively grouped and identified. However, as terminology relating to Audio Limiters varies, a brief description of control functions and typical use situations follows.

3.1.2 INPUT GAIN

With this control in the OdB position, overall circuit gain is unity. With the limiting controls set to restrict average and peak levels to appropriate values, the + gain positions of this switch will yield a positive overall circuit gain and corresponding degree of signal compression. - gain positions are generally used only to attenuate an input signal of a higher-than-nominal line level.

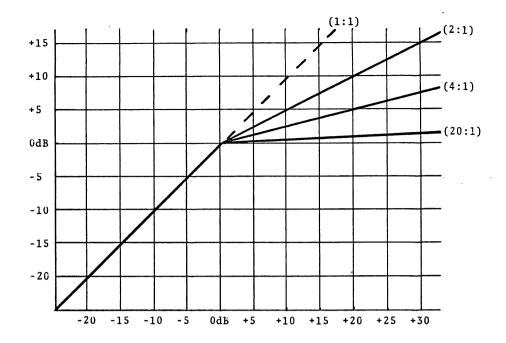
3.1.3 AVERAGE LEVEL LIMITER CONTROLS

In the NORM position, the MODE switch allows this limiter circuit to act as a quasi-VU responding gain control. This mode of operation achieves an effect similar to manual gain-riding based on VU meter indications. The maximum indication of a VU meter monitoring the Limiter output signal will correlate fairly well with the setting of the AVG. LIMIT control.

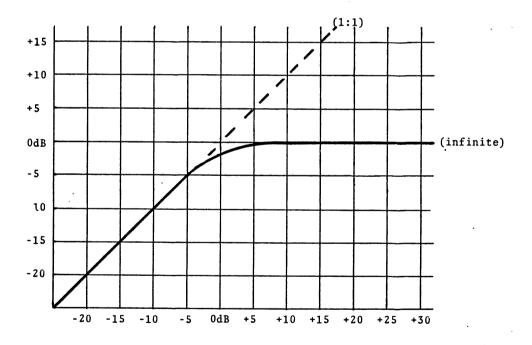
By setting the MODE switch to SLOW A.G.C., the normal function of the Average Level Limiter is preserved, but in addition a very slow-responding circuit corrects gain for long-term level variations. This mode is generally used with a certain degree of circuit gain (+ INPUT GAIN) to maintain a constant average level.

3.1.4 PEAK LIMITER CONTROLS

Unlike conventional Limiters operating in a closedloop configuration, the "knee" of the Inovonics Model 200 Limiter curve is not abrupt (see Fig. 3-1); rather, it is a gentle transition from a linear to a limited condition.



Conventional (closed loop) Limiter



Inovonics Model 200 Limiter

Figure 3-1
Comparison of Conventional Limiter and Inovonics Model 200 Transfer Curves

The small amount of increasing-ratio compression prior to the infinite ratio afforded by the optimally-flat ceiling of the Model 200, decreases the audibility of Limiter operation.

In the NORM position of the MODE switch, the PEAK CEILING control sets the absolute upper limit of program peaks; even those of such short duration as to be unmeasurable by conventional VU meters. The setting of the PEAK CEILING control is dictated by the dynamic range capability of the recording or transmission system (ie. 100% modulation of an RF carrier, groovewall breakdown of a phonograph disc, or a maximum permitted distortion in the case of a tape recording). The NORM position of the ATTACK switch gives fastest operation, assuring reduction of even the shortest-duration peaks. The DELAYED position may be used when very fast transients are subsequently clipped, or can otherwise be tolerated. The NORM position of the RELEASE switch is the best compromise between a fast recovery and low signal distortion, while the FAST position returns circuit gain to the unlimited value very quickly at the expense of a certain degree of low frequency signal distortion. Nevertheless, the unique distortion-reducing circuits of the Model 200 permit much shorter release times than those of conventional I.C. for a given value of distortion.

3.1.5 PEAK HOLD OPERATION

With its MODE switch in the PEAK HOLD position, the Peak Limiter section functions as a sample-and-hold circuit, or can actually be considered a Peak Limiter with infinite release time. After setting the CEILING control to the desired value of the highest program peak, a musical selection may be played into the Model 200, which automatically adjusts its gain to reduce the highest program peak to the preset ceiling value.

The musical selection can then be rewound (with tape lifters operated, of course), replayed through the Limiter into a second recorder, and dubbed at the automatically—adjusted, constant level. The highest program peak will remain at the ceiling value, but the dynamic range of the recording will be preserved, as no further gain change occurs during the dubbing process. PEAK HOLD operation is generally done with the Average Limiter OFF and the Peak Limiter ATTACK switch in the NORM position. The PEAK HOLD circuit may be reset by momentarily returning the MODE switch to NORM.

3.1.6 GAIN REDUCTION INDICATORS

The LINEAR lamp remains lighted as long as no gain reduction is in effect. The AVG. LEVEL REDUCTION lamp signals any operation of the Average Level Limiter circuit, and the PEAK LIMIT lamp lights whenever program peaks are reduced to the ceiling value. In the case of PEAK HOLD operation, this lamp lights when circuit gain is reduced, and remains lighted until the circuit is reset.

3.2 CIRCUIT DESCRIPTIONS

3.2.1 The Signal PCB contains all elements in the audio signal path. ICl is the input amplifier, and is associated with the INPUT GAIN control. The output of this stage is routed to both the AVG. LEVEL LIMIT and PEAK CEILING attenuators, and hence to the Control PCB. The output of ICl also feeds the Gain Reduction Module. This encapsulated circuit element provides the required gain reduction for Limiter operation as a function of a DC control current. The Module output drives Ql and Q2, the Class AB output stage. Diodes CR7 and CR8 provide output short circuit protection.

Negative DC control voltage from the Control PCB is fed to IC2, a unity-gain, FET-input buffer. This

LINEARITY control, R7, converts the voltage output of IC 2 to a proper current for linear gain reduction. The output of IC 2 is also inverted, by IC 3, AC-coupled through C6, and clamped by CR2 and CR4. This signal is fed out of phase with the gain controlling current to the Gain Reduction Module. The purpose of this circuit is to null the DC control signal ripple component and substantially reduce the generation of harmonic distortion, particularly at low frequencies.

3.2.2 Signals from the Peak Limiter CEILING attenuator are fed to the Control PCB, and to emitter follower, Q1. From Q1, the signal isspassed to a full wave rectifier circuit consisting of IC1, IC3, and related components. This rectifier circuit converts program peaks of either polarity to negative-going signals. Transistor Q3, a current gain stage, capacitor C9, and resistors R20, as well as those associated with the RELEASE switch, provide the desired Peak Limiter time constant. Diode CR13, one element of an analog "or" gate, couples the resultant DC voltage to the Signal PCB. IC5 and transistor Q4 drive the PEAK LIMIT indicator whenever the Peak Limiter is called upon to reduce circuit gain.

Similarly, signals from the AVG. LEVEL LIMIT attenuator are routed through emitter follower Q2 to a second full wave rectifier circuit, consisting of IC 2, IC 4, and related components. Capacitor C7, in this case, however, integrates the rectified signal to yield a negative voltage which represents the average, rather than the peak value of the input signal. In the SLOW A.G.C. mode, R17 and C8 perform a second, long-term averaging function. CR14, the second element in the analog "or" gate, feeds this DC signal to the Signal PCB. IC 6 and Q5 drive the AVG. LEVEL REDUCTION indicator. Transistor Q6 lights the LINEAR indicator when no gain reduction is in effect.

SECTION 4.0 ALIGNMENT AND CALIBRATION

4.1 GAIN CALIBRATION

With the INPUT GAIN attenuator set to OdB, and the PEAK CEILING and AVG. LEVEL LIMIT controls OFF, feed a nominal line level signal (+4 or +8dBm) of 500Hz to the Limiter input. Adjust GAIN CAL control, R16 on the Signal PCB, for an identical reading at the Limiter output. If the Limiter is to feed a terminated input, load the unit with a 600 ohm resistor at this time.

4.2 LINEARITY ADJUSTMENT

With the INPUT GAIN control set to OdB, and the AVG. LEVEL LIMIT control OFF, set the PEAK CEILING control to OVU, ATTACK, RELEASE, and Peak Limiter MODE switches to NORM. While monitoring the Limiter output with a VTVM, feed a 500Hz signal to the input. Increase the oscillator amplitude slowly. At some point the PEAK LIMIT indicator will light, and the output signal should stop increasing, even though the input signal is increased. If the output continues to increase, turn the LINEARITY control, R7 on the Signal PCB, counterclockwise. If the output increases to a point and then decreases as the input level is raised, turn the control clockwise. The proper adjustment of this control will yield a curve similar to the "infinite" curve plotted in Fig. 3-1. An optimallyflat ceiling will actually drop about 0.5dB when the input level is raised 15 to 020dB above the ceiling value.

4.3 PEAK LIMITER CALIBRATION

With controls set as in 4.2, feed the Limiter input with a 500Hz signal at a level 10dB above 0VU (oscillator output at +14 or +18dBm). Adjust the PEAK LIMIT CAL control, R15 on the Control PCB, for a Limiter output of 0VU (+4 or +8dBm).

4.4 METER CALIBRATION

If the optional remote meter is employed, it may now be

calibrated to read 10dB of Gain Reduction with conditions as in 4.3. Use the METER CAL control, R1 on the Signal PCB.

4.5 DISTORTION NULL ADJUSTMENT

Set the Peak Limiter RELEASE switch to FAST, and the test oscillator frequency to 50Hz. Other control settings and levels should remain as in 4.3. Monitor the Limiter output with a Total Harmonic Distortion Meter and adjust the DISTORTION NULL trimmer, R10 on the Signal PCB, for a minimum reading.

4.6 AVERAGE LIMIT CALIBRATION

Turn the CEILING control to OFF. aSets the tAVG. LEVEL LIMIT control to OVU, and Average Limiter MODE switch to NORM. Feeding the Limiter input with a 500Hz signal 10dB above OVU, adjust the AVG. LIMIT CAL control, R16 on the Control PCB, for a OVU output reading.

This completes calibration of the Model 200 Limiter.

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
	107300A	CONTROL PCB (SCHEMATIC 109800B)		
	2602	Transistor, Pads	Jermyn	TO5-001
C 1,2	0901	Capacitor, 5 uF, 25 V	Sprague	TE 1202
C 3-6	0801	" 10 pF, mica	Elmenco	DM15-100J
C 7	1051	" 2.2 uF, 35 V tantalum	Kemet	K2R2C35K
C 8,11	1052	" 22 uF, 35 V tantalum	Kemet	K22C35K
C 9	1050	" 4.7 uF, 35 V tantalum	Kemet	K4R7C35K
			y Y	
C 10	0803	Capacitor, 22 pF, mica	Elmenco	DM15-220J
	2 4			
CR 1-19	1100	Diode, Silicon, 1N4009	Fairchild	
IC 1-4,6	1300	Integrated Circuit, Type 748	Signetics	5748V
IC 5	1302	" Type LH0042	National	LH0042CH
				~
Q 1,2,6	1204	Transistor, 2N3567	National	
Q 3,4,5	1205	" 2N3645	National	
		(parts list 1)		
1 10000	1		I .	l

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SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	N					MFG.	MANUFACTURER PART NUMBER
	107300A	CONTROL PO	B B	cont-	16 112000A	i .			
R 1,2,20	0161	Resistor,	, 4W ,	10%,	1K				
R 3,4	0168	99	₩,	10%,	3.9K				
R 5-10	0089	99	¼W,	5%,	20K				
R 11,12	0083	11	₹W,	5%,	10K				
R 13	0177	99	¼₩,	10%,	22K				
R 14	0181	90	₹W,	10%,	47K				
									,
R 15	0563	Resistor,	Vari	able,	100K			Beck/Helipot	91A 100K
R 16	0564	99		2	200K			Beck/Helipot	91A 200K
R 17	0187	Resistor,	₫W,	10%,	150K			g	
R 18	0185	99	₹W,	10%,	100K				•
R 19	0197	**	₹W,	10%,	1 meg				
R 21	0180	**	₹W,	10%,	39K				
R 22-25	0176	99	₹W,	10%,	18K				
R 26	0375	99	½₩,	10%,	180 ohms		is a		100.
R 27	0379	98	½₩,	10%,	390 ohms				
R 28	0372	98	½₩,	10%,	100 ohms				
				(parts	s list 2)				

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
	106900A	SIGNAL PCB ASS'Y (SCHEMATIC 109400B)		
	2602	Transistor, Pads	Jermyn	TO-001
	109100	Gain Control Module		
C 1	0870	Capacitor, 0.47 uF, 200 V	Sprague	225-P47492
C 2,5	0803	" 22 pF, mica	Elmenco	DM15-220J
C 3	0810	" 100 pF, mica	Elmenco	DM15-101J
C 4	0801	" 10 pF, mica	Elmenco	DM15-100J
			ì	
C 6	0901	" 5 uF, 25 V	Sprague	TE 1202
C 7	0904	" 25 uF, 25 V	Sprague	TE 1207
CR 1-8	1100	Diode, Silicon, 1N4009	Fairchild	•
IC 1,3	1300	Integrated Circuit, Type 748	Signetics	5748V
IC 2	1302	" Type 536	Signetics	NE536T
Q 1	1204	Transistor, 2N3567	National	
Q 2	1205	Transistor, 2N3645	National	
		(parts list 3)		

SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	1	MFG.	MANUFACTURER PART NUMBER
	106900A	SIGNAL PCB	ASS'Y cont-		
	109100	Gain Cont	rol Module		
R 1,10	0559	Resistor,	Variable, 10K	Beck/Helipot	91A 10K
R 2	0078	**	¼W, 5%, 6.2K		
R 3	0185	**	¼W, 10%, 100K		
R 3	0180	11,	w, 10%, 39K (used when input tran	sformer is specif	ied)
R 4	0161	***	¹₄W, 10%, 1K		
R 5,11	0169	99	¼W, 10%, 4.7K		
R 6,8	0173	99	¹₄w, 10%, 10K		
R 7	0560	Resistor,	Variable, 20K	Beck/Helipot	91A 20K
R 9,12,13	0168	81	¹₄W, 10%, 3.9K		
R 14,15	0137	89	¼W, 10%. 10 ohms		
R 16	0558	Resistor,	Variable, 5K	Beck/Helipot	91A 5K
	5 5				
			(parts list 4)		

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SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
,	110300A	POWER SUPPLY PCB ASS'Y (SCHEMATIC 109900A)		
•	2600	Heat Dissipating Fins	Wakefield	207-AB
	2602	Transistor Pad	Jermyn	TO5-001
		•	Sprague	TE 1207
C 1,2	0904	Capacitor, 25uF, 25V	Sprague	TE 1202
C 3,4	0901	Capacitor, 5uF, 25V		
CR 1-4	1125	Rectifier, Silicon, 600V, 1A	Motorola	1N4005
CR 5,6	1101	Diode, Zener, 22V, 5%	Motorola	1N5251B
•			RCA	
Q 1 .	1212	Transistor, 40319	National	
Q 2	1204	Transistor, 2N3567	National	
Q 3	1205	Transistor, 2N3645	RCA	
Q 4	1200	Transistor, 2N2102		
R 1,2	0165	Resistor, ¼W, 10% 2.2K		
R 3,4	0169	ee ee 4.7K		
		(parts list 5)		
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SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
		CHASSIS (SCHEMATIC 110600A)		
C 1,2	0910	Capacitor, 500 uF, 50 V	Sprague	TVA 1315
F 1	2702	Fuse ½A 3AG		
I 1	2002	Indicator, Amber	Dialco	507-3918-1433-600
I 2	2001	" Red	Dialco	507-3918-1431-600
I 3	2010	" Green	Dia1co	507-3918-1432-600
·	2003	Retainer	Eldema	Q-081-905
	2004	Rubber Washer	Eldema	Q-145-008
				·
R 50	0180	Resistor, ¼W, 10%, 39K		
R 51	0173	" ½W, 10%, 10K		
s 1	117000	Cook to be a subtract and a TVT		
	117200	Switch Assembly, AVG LIMIT		
	117300	" INPUT GAIN		
	117400	" CEILING		7201 11
S 4	1807	Switch, DPDT min Toggle	C & K	7201 – H
		(parts list 6)		

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SCHEMATIC REF. NO.	PART NUMBER	DESCRIPTION	MFG.	MANUFACTURER PART NUMBER
		CHASSIS (SCHEMATIC 110600A)		
S 5,6,7	1804	Switch SPDT min Toggle	C & K	710 1- H
s 8	1808	Switch SPST Toggle Cu	tler-Hammer	7580 – K6
			·	
т 1	109000	Transformer, OUTPUT		
т 2	1502	Transformer, INPUT (optional)	UTC	0-37
	1503	Shield for T2	UTC	0-17
т 3	1501	Transformer, POWER	Triad	F-90X
				·
		(parts lists 7)		