OPERATING & MAINTENANCE INSTRUCTION MANUAL

MODEL 255

TRIBAND AUDIO PROCESSOR

INOVONICS
INCORPORATED

USER'S RECORD

Model 255 - Serial No. ......
Date Purchased ....
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INSTRUCTION MANUAL

MODEL 255

STEREO BROADCAST AUDIO PROCESSOR

July, 1987

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I FUNCTIONAL DESCRIPTION

Inovonics' 255 is a multifunction stereo audio processor for radio broadcast use. It was specifically developed to meet the challenges imposed by program material from digital audio sources in broadcasting systems which employ transmission preemphasis. This includes not only conventional FM stereocasting, but AM practices which follow the preemphasis/cutoff standard proposed by the U.S. National Radio Systems Committee (NRSC).

The Model 255 performs three separate processing functions: slow, "gain-riding" A.G.C., average-value level compression, and program peak control. The net combination is a processing system which delivers a very consistent level to the transmitter despite both long- and short-term program source level variations.

Feedforward gain control techniques using Pulse-Width-Modulation (PWM) are employed exclusively in all sections of the 255. The resultant control over processor action is unusually smooth, allowing a far greater amount of dynamic control to be called into play without audible degradation than permitted by more conventional feedback-mode VCA designs.

Particular emphasis has been placed on the flexibility of user control over the "subjective" processing parameters. An ample array of adjustments enables the user to control program "loudness" and "density" over a range adequate to suit nearly any programming format and personal taste. The 255 easily provides the aggressive processing demanded by today's "contemporary" music formats.

This manual is divided into several sections to best present the features, design philosophies, installation and operation of the Inovonics 255. Many of the specifications, and most of the operating instructions, are expressed in the manual text rather than in the more usual tabular form. It is recommended that the user at least skim Sections I, II and III before placing the 255 in service.

Automatic Gain Control (A.G.C.)

The output program mix from an audio console will invariably have long-term level variations from any of a number of sources. This problem might be attributed to inattention by the board operator, especially in a "combo" situation with more pressing duties than consciencious gain-riding. Notwithstanding this possibility, one major cause of level inequalities stems from the manner in which different operators respond to the level meter. Yet another, and more insidious reason, is the manner in which the level meter, itself, responds to music and voice.

The "VU" meter was developed for the broadcast industry. Though it has been in use for about fifty years, a number of factors have changed since the original specification was written. Through the 1950's, radio entertainment consisted mostly of speech and recorded symphonic or "popular" music which, because of the state of audio science at the time, had a restricted and predictable dynamic range and average-to-peak ratio. Today's music and recording techniques and audio technology yield much higher average/peak ratios. These are not accurately represented by the "sluggish" VU meter.

In European practice, and in "enlightened" domestic recording and broadcasting facilities, audio levels are based on the indication of a quasi-peak-responding "Peak Program Meter." The PPM provides a much more accurate display of program dynamics in terms of system headroom and overload margin. For this very reason, the slow A.G.C. stage of the Inovonics 255 employs the same 10-millisecond-integration peak response characteristic of the UK/EBU-standard PPM. The correction rate, on the other hand, is very slow and unobtrusive. This slow input level correction approximates manual gain control and does not audibly compress or otherwise alter program dynamics. It does, however, present the subsequent triband processing stages with a constant level based on program peak content.

To inhibit unnecessary "hunting" in the absence of program, the A.G.C. circuit is "gated." During brief pauses, gain is held at the last-corrected value until the program returns. For extended signal loss, gain is returned to a 0dB, unity-value figure at a rate somewhat slower than that for level correction. The gating circuit is frequency-weighted to recognize only legitimate program material. This prevents the A.G.C. from bringing up studio noise during pauses in an interview, for example. The gating control channel samples L+R energy with -3dB points at 150Hz and 5kHz. Threshold sensitivity is scaled to open the gate when the L+R midband program energy exceeds -25dB relative to nominal, corrected program "zero" level.

LEFT and RIGHT A.G.C. gain is under common control to preserve stereo image. Gain is established by sampling both channels independently and acting on the higher level. The A.G.C. is defeatable as might be desired with classical music, or when the 255 is preceded in the audio chain by some other leveling device. Defeating the A.G.C. function is described on Page 14.

Triband Spectrum Division

Following the slow A.G.C. stage, the program audio is split into three frequency bands as graphed in Figure 1. The LOW and MID bands have a crossover at 200Hz. This isolates "low bass" frequencies into a channel of independent control. High energy, low frequency program components (such as a "kick" drum) which reach 100% modulation will reduce gain in only the LOW band and won't "punch holes" in the MID and HIGH regions, or otherwise sacrifice program loudness.

The MID/HIGH crossover follows (and protects) the transmission preemphasis curve. This is selectable for either the 50- or 75-microsecond, or, alternately, a "flat" transmission characteristic when preemphasis protection is not a consideration. MID/HIGH crossover selection is explained on Pages 13-14.

Independent high frequency gain control performs a dual function. First, it restricts program energy which would otherwise violate the modulation constraint imposed by the system preemphasis characteristic. Also, and in a manner akin to the LOW band gain reduction circuit, high energy, high frequency program peaks (such as cymbals, strong sibilants, etc.) which reach 100% modulation will be quickly and independently controlled without sacrificing modulation in the predominant MID band.

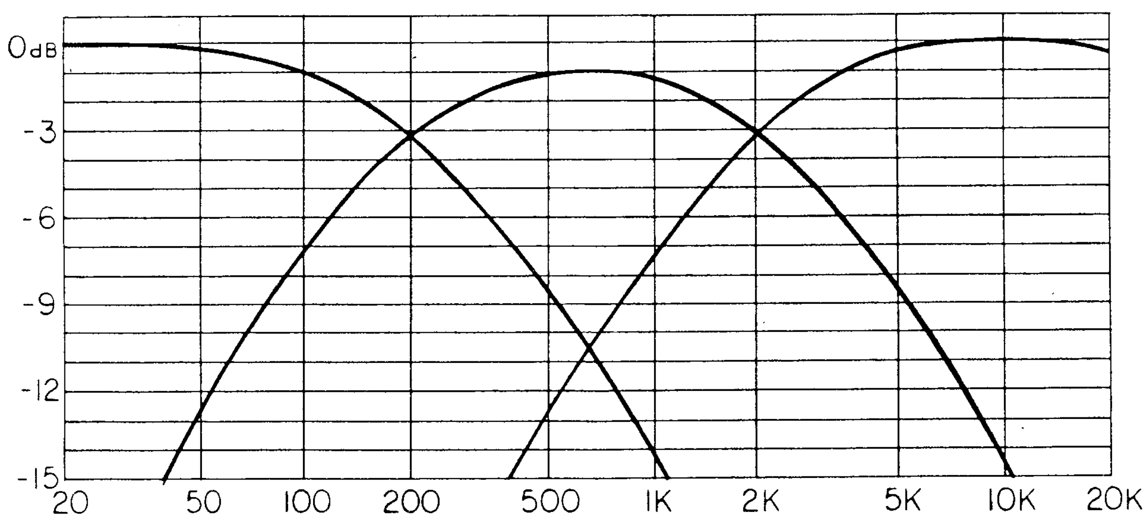


Figure 1 - TRIBAND FREQUENCY DIVISION

Triband frequency division employs gentle, "natural function" 6dB-per-octave crossovers derived from a two-step signal subtraction process. This method eliminates peaks and dips at the crossovers during dynamic reduction, and ensures overall flat response whenever the three bands are recombined at unity gains as in the "PROOF" mode.

"Dynamic Reduction" Defined

Average level compression and peak limiting share common gain control circuits in each of the three frequency bands. The two functions are separated by a variable, time-domain "floating platform" attack/release characteristic. Because the 255 is a frequency-discriminate processor, attack and release timing may be optimized in each band, and also made variable for user control over subjective results.

Two control channels are derived from the MID band program energy. One is based on the instantaneous value of the program signal in that band and is responsible for actual MID band Dynamic Reduction. The other is an averaged, or integrated control channel representing the mid-frequency, quasi-average program level. It is from this "average" level representation that the variable "platform" is derived for all three bands.

An occasional MID band program peak will add little to the integrated platform level. Repetitive peaks, on the other hand, will constitute an increase in the average value of the signal. Thus the program dynamics (average/peak ratio) establish the basis for a working platform-to-peak differential.

Each band has, in effect, a dual release timing: a fast initial release from peak reduction to that of the average (platform) level, followed by a slower "platform release" for the average level. The user is provided with adjustments which directly, or indirectly, affect peak and average release timing in all three bands. The subjective effects of these adjustments are detailed under SETUP AND OPERATION, Section III.

The average-value "platform" level is gated in much the same manner, and by the same gating circuitry, as the slow A.G.C. stage.

In the absence of a program signal, the platform will slowly seek a -6dB "resting" value. This is a more-or-less arbitrary number, but supposes that program average level gain reduction will be maintained somewhere near this figure. In actual operation, the platform will remain within the range which has been selected by the user.

During brief pauses in the program, the platform will be held at its last value. Platform release to full gain (0dB G/R) is temporarily inhibited to prevent rush-up of background noise. Extended program loss will cause the platform to return very slowly to the -6dB "resting" point.

Dynamic Reduction gain control is accomplished with a feedforward technique employing Pulse Width Modulation. A brief "tutorial" on PWM is included with the CIRCUIT DESCRIPTIONS in Section IV.

An advantage of feedforward gain control over the more conventional feedback techniques is the ability to tailor the input-to-output G/R transfer characteristic for smoother-sounding processor action. The transfer characteristic of the Model 255 triband circuitry is graphed in Figure 2. It is a "soft knee" function with an area of increasing-ratio compression prior to the infinite, final limiting ratio.

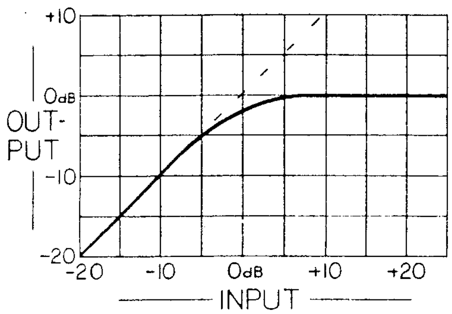


Figure 2

DYNAMIC REDUCTION TRANSFER

CHARACTERISTIC (Input vs. Output)

LEFT and RIGHT Dynamic Reduction is under common control in all three bands to preserve the stereo image. Gain reduction is based on the higher of the LEFT or RIGHT program channels.

"Spectral Loading" Feature

"Spectral Loading" refers to the natural result of multi-band audio processing in which no means of inter-band control correlation is employed. For example, in a 3-band, totally discriminate system, 10dB of midband gain reduction would not necessarily cause a similar reduction in either the low or high bands. The result is a 10dB artificial boost of any low energy, low and high frequency program component: "dynamic skewing" of the system response. While this processing artifact might be deemed desirable for increasing spectral density, it will invariably impart an unnatural and, perhaps, unwanted "busy" character to the program. Also, program material which is not completely "clean" will have any inherent noise or distortion accentuated.

One of two methods is commonly used to obviate this problem. Either a fixed amount of midband audio is bled into the "sidechains" of the other two bands, or the midband DC control signal is combined with that of the other bands.

The Model 255 utilizes a common average-level "platform" for all three bands derived from integrated midband program energy, and separate from the midband gain reduction control signal. Moreover, the user is given control over the LOW and HIGH band platform values to vary the "low-end enhancement" and "brightness," respectively. (See Section III)

Program-Adaptive Clipping and "H.F.A.D."

A unique feature of the 255 takes advantage of the psycho-acoustic phenomenon of "masking" to reduce certain audible effects of heavy processing. This feature is especially useful in controlling the high frequency energy so abundant in digitally-recorded music.

A "High Frequency Activity Detector" monitors program dynamics at the upper frequencies to determine an optimum limiting/clipping ratio for both the MID and the HIGH bands. When there is little high frequency dynamic activity, the peak control function of the MID and the HIGH bands operates as a low-distortion, true limiter. When sufficient high frequency activity is present to mask otherwise-audible effects, the peak control function reverts to increased clipping of the very fast peaks for less sacrifice of program "brightness" at higher values of gain reduction.

Action of the H.F.A.D. is monitored by a LED indicator under the removable front cover of the 255. If desired, the Program-Adaptive Clipping function is easily defeated as described on Page 15.

"Safety" Clipper

An active "safety" clipper follows the triband Dynamic Reduction stages. This clipper does not normally act on program material, but guards against certain fast overshoots which can occur when the independently-limited bands are recombined. Like the triband circuitry, the "safety" clipper also follows the selected preemphasis-protection frequency characteristic.

Unlike conventional "hard" clippers, the "safety" clipper of the 255 is integral with the PWM circuitry, working in a fashion silmilar to an "RF" clipping circuit. Clippers of this type are credited with substantially lower harmonic and intermodulation distortion.

"PROOF" Mode

In the "PROOF" mode, the audio signal path remains intact through all processing stages, but the Slow A.G.C. and Dynamic Reduction gain-control functions are defeated. A.G.C. gain is fixed at 0dB, and gains in the three frequency bands slowly return to the -6dB "resting" value.

Specifications

Tabulated below are the Model 255 performance specifications which are not specifically expressed in the text of this Manual, depicted in the drawings attendant to the text, or glaringly obvious from cursory examination of the 255 itself.

Frequency Response (in "PROOF," or below Dynamic Reduction threshold): +/-0.5dB, 10Hz-20kHz.

Noise: Better than 80dB below 100% modulation, 10Hz-20kHz.

Distortion (with full A.G.C. correction, "subjective" adjustments centered, and with 10dB of Dynamic Reduction): <0.25% THD, 1kHz-20kHz; <0.5% THD, 250Hz-1kHz; <1.0% THD, 25Hz-250Hz.

Crosstalk: Better than -65dB, 10Hz-20kHz.

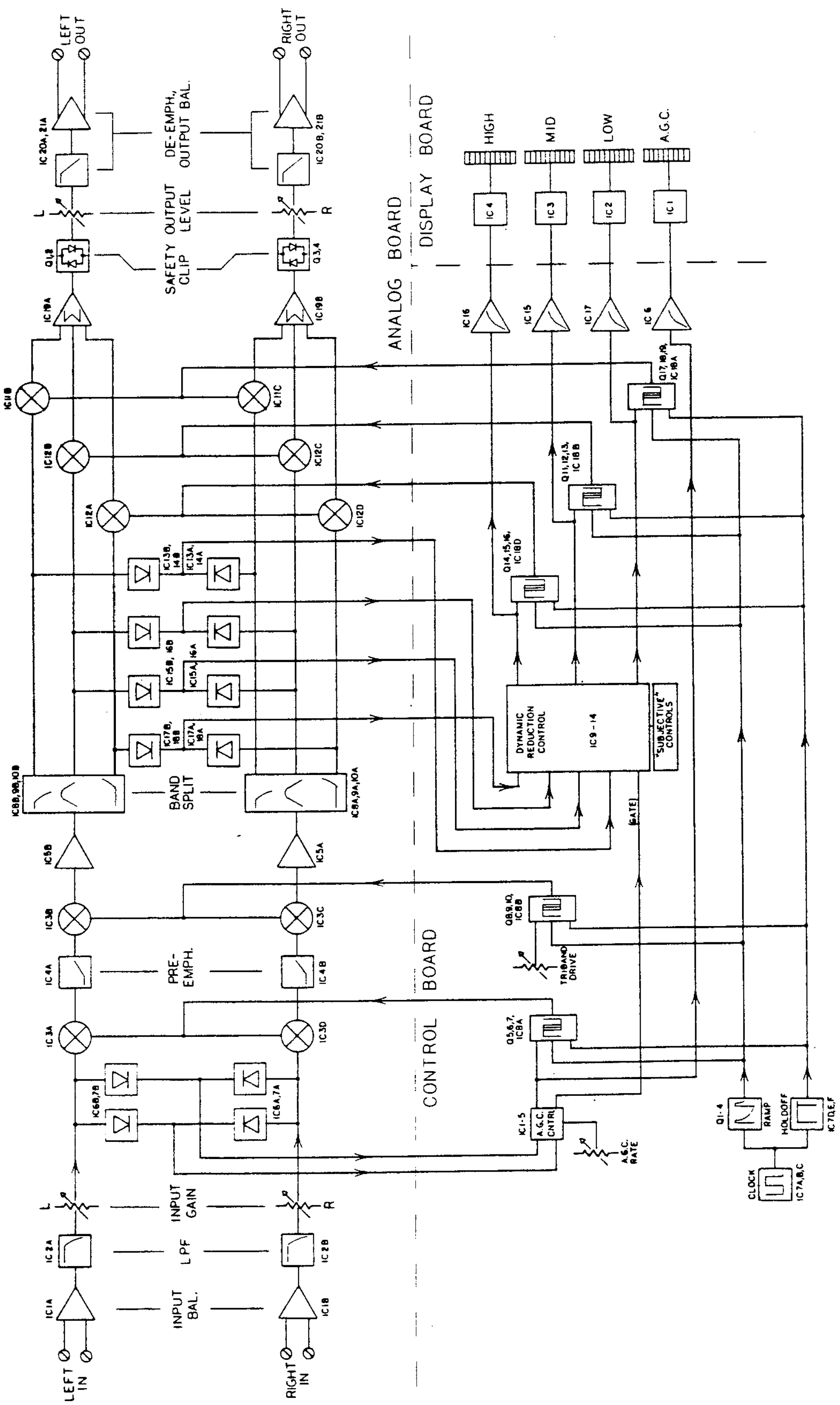
Inputs (LEFT and RIGHT): Active-balanced, 10K-bridging; accept nominal line levels between-20 and +10dBmV.

Outputs (LEFT and RIGHT): Active-balanced, 600-ohm resistive source impedance; deliver 0dBm to +15dBm into 600-ohm loads.

Power Requirements: 105-130 or 205-255VAC, 50/60Hz; 12 Watts.

Size: 3-1/2" x 19" x 7" (2U).

Shipping Weight: 9 lbs.



<u>Figure 3</u> - BLOCK DIAGRAM, MODEL 255

II INSTALLATION

Unpacking and Inspection

Upon receipt of the equipment, inspect carefully for shipping damage. Should any such damage be observed, notify the carrier at once; if not, proceed as outlined below. It is recommended that the original shipping carton and packing materials be retained should future reshipment become necessary. In the event of return for Warranty repair, shipping damage sustained as a result of improper packing for return may invalidate the Warranty.

> IT IS VERY IMPORTANT that the Warranty Registration Card found at the front of this manual be completed and returned. Not only does this assure coverage of the equipment under terms of the Warranty, and provide some means of trace in the case of lost or stolen gear, but the user will automatically receive specific SERVICE OR MODIFICATION instructions should they be issued by the factory.

Mounting

The Inovonics 255 is packaged to mount in a standard 19-inch equipment rack and requires only 3-1/2 inches (2U) of vertical rack space. The 255 generates negligible heat, and itself is unaffected by wide variations in the ambient operating temperature.

AC Power

Unless specifically ordered for export shipment, the 255 is set to operate from 125V, 50/60Hz AC mains power. The back-panel designation next to the fuseholder will confirm both the mains voltage selected and the value of the fuse to be used.

Mains voltage reselection is easily made with the 255 top cover removed. A plug-on jumper strip next to the power transformer may be installed in either of two positions for the two nominal mains voltages. A silkscreened legend next to the connector clearly indicates orientation. A proper fuse must be installed, and the appropriate back-panel voltage designation marked to indicate the input power requirement.

The power cord supplied with the unit is fitted with a North American standard male connector, but the individual cord conductors are <u>supposedly</u> color-coded in accordance with CEE standards: BROWN = "hot," BLUE = neutral, GREEN/YELLOW = ground. If this turns out <u>not</u> to be the case, U.S. color coding applies: BLACK = "hot," WHITE = neutral, GREEN = ground.

<u>RFI</u>

Though the 255 has been designed to operate in close proximity to broadcast transmitters, care should be exercised in locating the unit away from abnormally high RF fields.

In some installation situations, an RF ground loop may be formed between the input or output cable shield grounds and the AC power cord ground. Use of a "ground-lifting" AC adapter should remedy the problem. The chassis of the unit must somehow be returned to earth ground for safety.

<u>LINE INPUTS and Range Selection</u>

The Model 255 has separate LEFT and RIGHT electronically-balanced (transformerless) bridging LINE INPUTS. These are brought out to the rear-panel barrier strip and include a chassis ground connection for cable shields.

Should the equipment which <u>feeds</u> the Processor require output loading, a 600-ohm terminating resistor may be placed across the 255 input terminals.

The "+" and "-" input terminal designations remain in-phase with LINE OUTPUT terminals similarly identified. If the 255 is fed single-ended (unbalanced), connect the "hot" signal lead to the "+" terminal, and strap "-" to "GND" for a common signal return lead connection.

The 255 accepts zero-reference input program levels between -20 and +10dBmV. This 30dB input level range is divided into two 15dB segments selected with a series of four jumpers next to the input barrier strip under the top cover.

As shipped, the 255 is preset for line input levels between -5 and +10dBmV. This is the "HIGH" range, and identified by the letter "H" silkscreened in two places next to each of the two sets of level range jumper connectors. For input levels between -20 and -5dBmV, the four jumpers must be moved to the "L" ("LOW" range) positions. Figure 4 on the next page shows the two input level range jumper placement options.

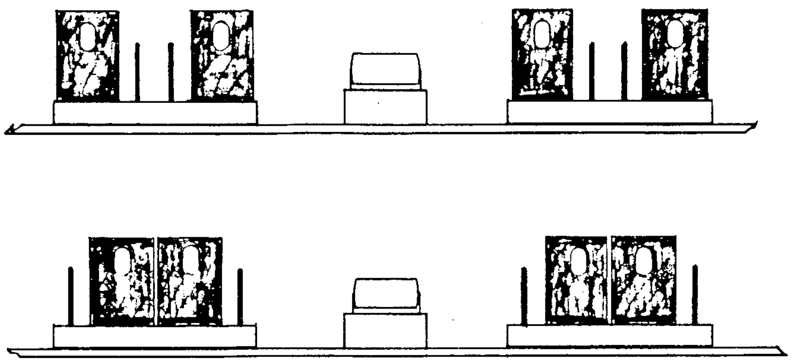


Figure 4 - INPUT LINE LEVEL RANGE SELECTION

LINE OUTPUTS

The LEFT and RIGHT LINE OUTPUTS appear at the rear-panel barrier strip along with ground terminals for cable shields. Outputs are electronically-balanced (transformerless), but are not load-sensing. They will drive balanced inputs of stereo generators and transmitters or balanced (ungrounded) studio lines.

If a single-ended unbalanced output is required, only the "+" and "GND" terminals should be used. Do NOT ground the "-" side of the output.

The characteristic, resistive output impedance of the 255 is 600 ohms. When terminated in a similar resistance, the output level will drop 6dB below the unloaded value. The outputs are variable between 0 and +15dBm into balanced, 600-ohm loads.

LINE OUTPUTS are designated "+" and "-" for program phase considerations, and are in-phase with the similarly-designated LINE INPUT terminals.

Preemphasis Characteristic Selection

The 255 output has a FLAT, not a preemphasized characteristic. System preemphasis is normally imparted by the stereo generator or transmitter.

The 255 does, however, provide preemphasis protection which can be selected to complement either the U.S.-standard 75-microsecond, or the European-standard 50-microsecond curves. A "zero" mode is included as well. This is used when the 255 is not required to provide preemphasis protection.

The three options are selected with a series of six jumpers under the top cover of the unit. Figure 5 shows the curve selection jumper options. A "0," a "50" and a "75" are silk-screened next to the appropriate terminals for identification. Unless designated for export shipment, the 255 is preset for the 75-microsecond curve.

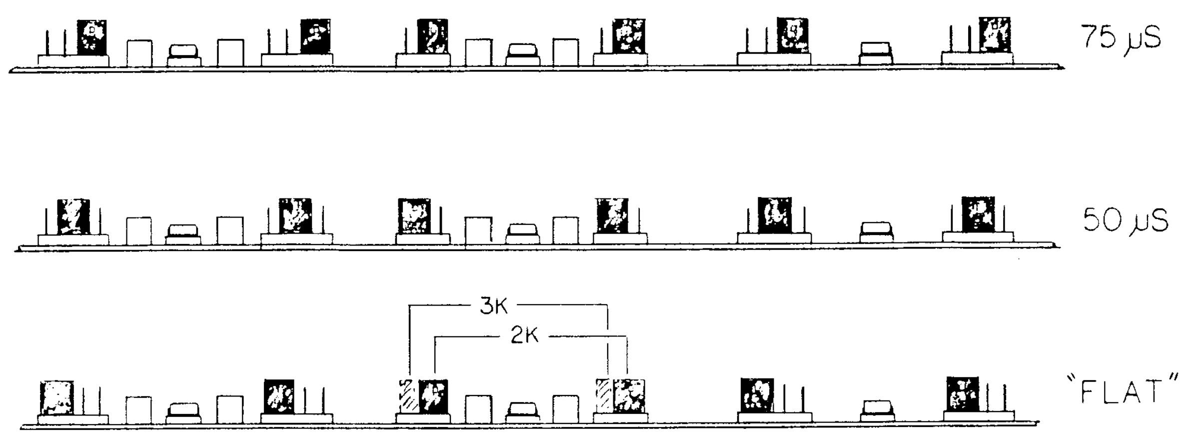


Figure 5 - PREEMPHASIS PROTECTION SELECTION

"Flat" Mode Operation

The Inovonics 255 finds certain application in studio and production situations where preemphasis protection is not required. This is also the case when the 255 is followed by some other frequency-selective limiter. In these instances, the "0" terminals are jumpered in the appropriate four places, leaving the two sets of terminals which have only the "50" and "75" designations. These set the MID/HIGH crossover frequency at 3kHz or at 2kHz, respectively, and may be jumpered at the user's option.

A.G.C. Defeat

The Slow A.G.C. function of the 255 may be easily defeated for those processing applications which either do not require initial "gain-riding," or, as in the case of classical music, when the long-term dynamic range of the program material wants to be preserved.

To locate the jumper which enables and disables the A.G.C. function, remove the top cover of the unit and look just behind the A.G.C. RATE control on the lower circuit board. The upper board does not have to be removed to access the jumper. The two positions for A.G.C. ON and OFF are clearly designated in the silkscreened circuit board legend.

Program-Adaptive Clipping Defeat

The unique Program-Adaptive Clipping feature of the 255 is very useful in reducing the audible effects of heavy processing, especially when dealing with program material rich in high frequency energy. Provision has been included to defeat this function so that the user can evaluate the utility of the feature for himself.

The jumper which defeats Program-Adaptive Clipping is on the main, lower circuit board, and the upper board will have to be removed for access to it.

Five screws must be removed to lift the upper circuit board up-and-out of the unit. These are the two screws which secure the barrier strip to the back panel, and three screws near the front edge of the upper board. When the upper board is lifted out, the two ribbon cables may be left connected and the processor operated in this condition.

The jumper which enables or defeats the Program-Adaptive Clipping feature is near the center of the area normally covered by the upper circuit board. The connector strip is designated "PAC" in the silkscreened legend, as are the ON and OFF jumper positions.

III SETUP AND OPERATION

Setup of the Inovonics 255 processor is very simple and straightforward. The only test equipment required is a 500Hz, sinewave signal source which can be routed through the audio console, and an AC voltmeter. Initial setup is performed with the Model 255 "on air" in the normal broadcast chain. The procedure assumes a combined studio/transmitter site with customary equipment interconnecton.

INPUT GAIN Set

STEP 1 Apply a 500Hz sinewave test signal to the LEFT input (only) of the processor from the audio console or from whatever other equipment directly feeds the unit.

STEP 2 Adjust the level of the test tone for a value exactly 1.5dB above the normal program "zero" level.

A. This would be +9.5dBm if 0VU= +8dBm; +5.5dBm if 0VU= +4dBm. A +1.5VU indication on the console meter is sufficiently accurate.

B. This would be 1.5dB above the "TEST" level if Peak Program Meters are used.

STEP 3 Adjust the LEFT INPUT GAIN control to a point which causes both the 0dB and the -3dB SLOW A.G.C. GAIN indicator LEDs to light evenly.

A. This step must be performed slowly because of the very slow A.G.C. correction rate.

B. If this adjustment is not within the range of the panel control, check the Input Range Selection procedure on Pages 12-13.

STEP 4 Remove the test signal from the LEFT input and apply it to the RIGHT input (only). Repeat STEP 2 and STEP 3 for the RIGHT channel.

STEP 5 Reduce the 500Hz test signal to nominal line level (0VU). The 0dB SLOW A.G.C. GAIN indicator should light for either a LEFT-only, a RIGHT-only, or a LEFT and RIGHT test signal input from the console.

OUTPUT LEVEL Adjustment

This procedure is most easily performed "on air" using the station Modulation Monitor and a 500Hz sinewave test signal from the audio console. Alternately, the OUTPUT LEVEL controls may be adjusted for a known, 100%-modulation output line level.

STEP 1 Apply a 500Hz, 0VU sinewave test signal from the audio console to the LEFT input (only) of the 255. If the INPUT GAIN Adjustment Procedure has been properly performed, the 0dB SLOW A.G.C. indicator will stay lighted.

STEP 2 Increase the 255 TRIBAND DRIVE control for 10dB of indicated MID-BAND DYNAMIC REDUCTION.

STEP 3 The LEFT OUTPUT LEVEL control is now adjusted for 100% transmitter modulation as indicated by the station Mod-Monitor, or for the known, 100%-mod output line level.

STEP 4 Remove the 500Hz test signal from the LEFT input and apply it to the RIGHT input (only) at the same level. Neither the SLOW A.G.C. GAIN nor the MID-BAND D/R should differ from the LEFT channel indications.

STEP 5 Adjust the RIGHT OUTPUT LEVEL control, either for 100% transmitter modulation per the Mod-Monitor, or for a proper line output level.

STEP 6 Drive both the LEFT and RIGHT channels with the test tone. Indicated D/R should remain at 10dB, and transmitter modulation at 100%.

"Subjective" Processing Adjustments

The array of seven adjustments beneath the removable front door of the Model 255 enables the user to exercise a good deal of control over the "sound" imparted to the processed program audio signal.

Typical, or "normal" operation may be assumed when all seven controls are at "12 o'clock" (straight up). In general, turning each control clockwise (CW) makes the processing more aggressive (LOUDER), and counterclockwise (CCW) gives more conservative results. A detail of each of the controls follows.

-- A.G.C. RATE --

This sets the correction rate for the slow, gain-riding A.G.C. function. Though it performs a slow level correction, the response of this circuit is to peak content of the program material per the UK/EBU integration specification. This presents subsequent processing stages with a signal which has a more uniform peak-weighted level.

Because the A.G.C. correction rate is slow in any case, there will be little, if any, audible difference in most program material whether this control is fully CW or fully CCW. 0.5dB/sec. (straight up) is about optimum, though formats which have more initial dynamic range ("beautiful music" and talk shows) could benefit from a slower (CCW) setting, and contemporary music with a more consistent average level a faster (CW) one.

-- TRIBAND DRIVE --

This adjusts the input level to the 3-band processing section, and also provides means to adjust processor static gain in the "PROOF" (bypass) mode. The setting of this control bears directly on the other "subjective" adjustments, as the effect they have over the program audio will, in turn, be increased or decreased by the amount of TRIBAND GAIN programmed into the system.

The setting of this control will, in most instances, correlate with the amount of midband peak Dynamic Reduction indicated by the LED display.

-- PLATFORM RATIO --

The setting of this control defines the number of dB below the typical value of peak Dynamic Reduction that the level of average reduction will be maintained. With the control fully CCW, the average program level is consistently reduced to a lower value, actually only a couple of dB apart from that of typical peak reduction. This preserves program dynamic range, but at the expense of less perceived loudness.

When the PLATFORM RATIO control is rotated fully CW, there can be as much as a 10dB differential between the peak and average reduction values. With "platform" G/R that much less than for peaks, overall gain will increase more quickly and to a higher value following a peak, and a higher average program level will result.

PLATFORM RATIO is the one adjustment most useful in controlling overall loudness, and in reducing any audible artifacts of heavy processing.

-- PLATFORM RELEASE --

This control adjusts the release time of the average level, Dynamic Reduction "platform." While the effect of this control is not nearly so dramatic as that of PLATFORM RATIO, it does have a subtle secondary effect over perceived loudness, and gives further means for reducing any audible side-effects of heavy processing.

-- SPECTRAL "LOADING" (LOW & HIGH FREQ.) --

As explained on Page 7, "loading" of the audio spectrum occurs when gain is decreased in the mid-frequency region without similar gain reduction in the other two bands. The primary utility of multiband audio processing is to reduce or eliminate "holes" in the predominant MID band, or "loudness" frequency range, when additional reduction is required at the top or bottom ends. Frequency extremes are generally credited with little contribution to perceived loudness.

The LOW FREQ. and HIGH FREQ. controls each regulate the degree to which the 255 will function as a frequency-discriminate processor. At the CCW, 0dB rotation, the average level "platform" value of the MID frequencies will control the other two bands on a one-for-one basis. This means that a 6dB "platform" value of average level reduction will cause 6dB reduction in the LOW and HIGH bands. Of course the LOW and HIGH bands may each reduce gain in excess of the MID band average figure should high energy in either or both bands demand more G/R than the MID.

As the LOW FREQ. and HIGH FREQ. controls are adjusted CW, LOW and HIGH band dependence on midband average energy is reduced accordingly, and an artificial, energy-dependent boost occurs in those bands. Moreover, the Dynamic Reduction release time is decreased simultaneously, which increases the signal "density" within the LOW and HIGH bands as well.

The amount of "loading" (or boost) in either the LOW or HIGH bands is restricted to a maximum of 6dB. Much more than this has been shown to audibly degrade the program signal rather than to offer any subjective improvement in "bottom" or "brightness."

-- MIDBAND DENSITY --

This control adjusts initial MID band release time for fast peaks to the average, "platform" value. It will have little effect when a low PLATFORM RATIO is maintained, but with a PLATFORM RATIO of 6dB or more, clockwise rotation of the MIDBAND DENSITY control will increase the energy in the dominant MID band region. When 3dB or more of LOW FREQ. or HIGH FREQ. SPECTRAL "LOADING" is used, the MIDBAND DENSITY should be adjusted CW to preserve the definition and intelligibility of vocals in contemporary music formats.

IV CIRCUIT DESCRIPTIONS

This section details the circuitry of the Inovonics 255. These discussions refer to the various pages of Schematic Diagrams contained in the Appendix, Section V, pages 36 through 41.

The first part of this Section covers the general subject of Pulse Width Modulation (PWM) and its implementation in the Model 255. Signal path circuitry discussions follow.

Pulse Width Modulation

PWM is utilized exclusively for audio gain control in the Inovonics 255. This quasi-digital approach is perhaps the most simple and "colorless" means of varying the amplitude of an analog signal with a DC control voltage.

Consider an audio signal which can be turned on and off with a toggle switch. When the switch is ON, attenuation is zero. When OFF, attenuation is infinite. If we satisfy the Nyquist sampling theory and are able to toggle this switch at a rate at least twice that of the highest audio frequency, linear signal attenuation becomes directly proportional to the OFF time.

ON	OFF	dB ATTEN
100%	0%	0dB
50%	50%	6dB
25%	75%	12dB
10%	90%	20dB
1%	99%	40dB
0%	100%	(infinite)

This technique gets a bit touchy at small duty cycles (40dB or more attenuation), relegating it to uses which do not require a great amount of gain reduction. PWM thus lends itself nicely to audio processing applications because it is easily implemented and very predictable over the 0 to 30dB range required.

The "clock" (switching) frequency used in the Model 255 PWM circuitry is 152kHz, a multiple (8X) of the FM "pilot." Since the clock is well above the Nyquist rate, no elaborate anti-aliasing filters are needed, either in the signal input stages or to remove the switching frequency from the output signal.

PWM Generation

Gain control circuitry in the 255 operates in a feedforward mode rather than in the more common feedback configuration. This necessitates a conversion function to cause a dB of output signal decrease for each dB that the input signal increases to hold the final output level constant.

Put into linear (voltage), rather than log (dB) terms, the function can be expressed simply as X = 1/Y. Figure 6 graphs this function for a case where X represents circuit gain (reduction) required to hold a 1 - 10-volt input signal, Y, at a constant, 1-volt output.

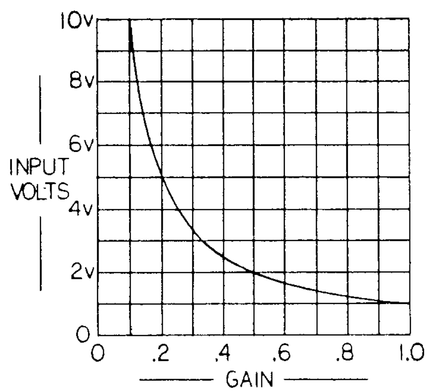


Figure 6

VOLTAGE TRANSFER FUNCTION

If we assume a linear relationship between PWM "OFF" time and signal gain reduction, the 1/Y expression translates directly to the duty cycle; i.e.: 0.1 = 10% "ON," and 1.0 = 100% "ON."

In actual implementation, however, we need a "threshold" level, below which gain will remain at full value. Just above threshold the function will conform to the desired "soft knee" characteristic (see Figure 2, Page 7). Above the gentle transition the X = 1/Y expression will fully apply. This final, "composite" function is graphed in Figure 7.

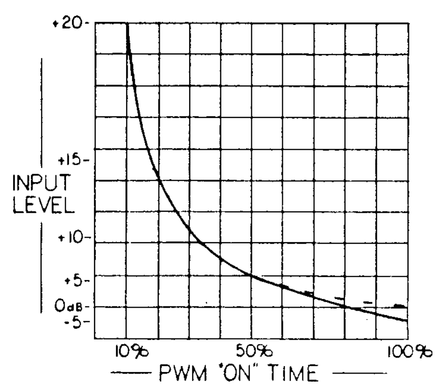


Figure 7

PWM DUTY CYCLE

VS. INPUT LEVEL

Clock and Ramp Generator

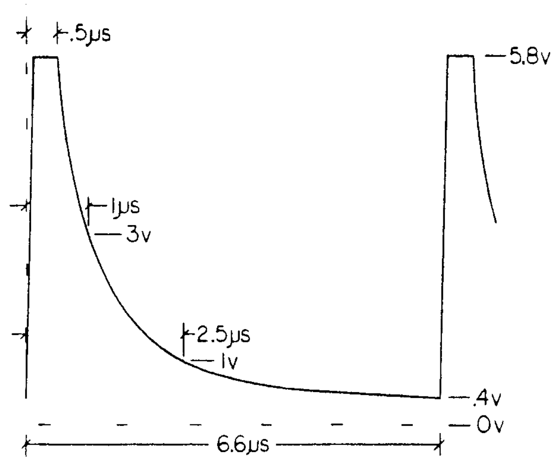
Referring to the Control Board Schematic on Page 39, IC7A and IC7B form a free-running multivibrator for the 152kHz "clock" frequency. TP1 may be monitored with a frequency counter, and the frequency adjusted with R48. This is the only calibration adjustment in the Model 255, and its setting is not at all critical.

With each positive transition of the clock, Q1 is momentarily turned off by a pulse through C9. This saturates Q2 and charges C10 to the +15V supply rail.

C10 has a "compound" R/C discharge time constant. As soon as Q2 turns back off, C10 discharges through R55, R56 and R57. When the discharge reaches the bias voltage level at the cathode of CR11, R56 is biased out of the circuit and the discharge assumes a slower rate. Similarly, when the ramp reaches the CR12 bias point, the only remaining path is through R55 and R61 to ground, and the discharge slows even more. The result is a "compounded" log ramp which closely follows the curve shown in Figure 7, but is repetitive at the 152kHz rate.

Clock pulses at TP1 are also differentiated by C8 to produce a 200-nanosecond "holdoff" pulse coincident with the charging of C10. This pulse may be observed at TP2; its purpose is described later.

The ramp waveform is buffered by Q3 and Q4. It is shown in Figure 8 and may be monitored with an oscilloscope at TP3. Accuracy of the feedforward transfer function depends directly on the integrity of this waveform, and both voltage levels and timing information are noted. Other "TP" monitor points are identified in the table next to Figure 8.



TEST POINT		DESCRIPTION
TP1	-	152kHz "CLOCK"
TP2	-	200ns "HOLDOFF"
TP3	-	"RAMP" WAVEFORM
TP4	-	T/B DRIVE PWM
TP5	-	A.G.C. PWM
TP6	-	MID-BAND PWM
TP7	-	LOW-BAND PWM
TP8	-	HIGH-BAND PWM

Figure 8 - "RAMP" WAVEFORM (TP3)

PWM-Generation Comparators

Q8, Q9 and Q10 form a discrete-component, high gain comparator circuit. This example is typical of five such circuits used to develop the actual squarewave PWM switching signals.

In this exapmle, a DC control voltage from the wiper of the TRIBAND DRIVE control is presented to the base of Q8. This particular control voltage may be varied from about 0.5V, for full TRIBAND DRIVE, to about 2.5V for minimum DRIVE. The ramp waveform is fed to the base of Q9, and each time the negative-going ramp crosses the control voltage level, the collector of Q10 toggles from +15V to -6V. this is translated to a +/-6V level at pin 6 of IC8B to be in keeping with the ground-referenced bipolar 6V operating range of all the CMOS logic circuitry in the gain-control portion of the processor.

In any of the comparator circuits, a lower DC control voltage will result in a longer PWM duty-cycle ON time. When the voltage drops to zero, as is the case when no signal gain reduction is required, the PWM waveform would normally revert to a constant +6V logic level. Therefore an AND gate (IC8B in this case) follows each comparator and combines the "raw" PWM with the 200-nanosecond "holdoff" pulse to maintain a finite OFF time and preserve the "switching" nature of the PWM waveform.

Signal Input Circuitry / Preemphasis

Referring to the Analog Board Schematic on Page 36, LEFT and RIGHT input signals feed an active input "balancing" stage, IC1. A section of the buildout resistance in each leg of the two inputs may be shorted with a jumper to increase gain for low level signals. This procedure is covered on Pages 12 and 13.

IC2 combines a third-order lowpass filter with a variable gain amplifier. The associated control adjusts INPUT GAIN over a 15dB range, and the filter removes any noise components from the input signal which might be "aliased" by the PWM switching frequency.

The outputs from IC2 are fed through CMOS switches to the "active" preemphasis amplifier, IC4. IC3A and IC3D are driven by the PWM squarewave from the TRIBAND DRIVE comparator. Gain at this point is manually variable over a range of approximately 15dB.

The active preemphasis circuits have a "tuned" response. Gain follows the selected 75- or 50-microsecond (or "flat") characteristic to just over 20kHz, at which point the stage assumes a second-order lowpass falling response to attenuate the TRIBAND DRIVE PWM switching component.

Slow-A.G.C. Stage

From IC4, program audio passes through CMOS switch sections IC3B and IC3C. These are driven by PWM from the A.G.C. comparator. Audio is recovered by lowpass amplifier IC5 to feed the subsequent triband processing section.

A portion of the LEFT and RIGHT program is routed from IC2 to a pair of full-wave, "precision" rectifiers, IC6 and IC7. The initial gain stages (IC6A and IC6B) include a pair of diodes in the feedback path to compensate for forward drop in the actual rectifier diodes. Further, the response of these stages is tailored to favor "legitimate" program energy as mentioned in the initial discussion of the gating circuit on Page 4.

The LEFT and RIGHT rectifier circuits are peak-responding. Four pairs of rectifier diodes are so interconnected that two, independent outputs are created, each responding to the highest peak value of either the LEFT or the RIGHT channel.

A.G.C. control, gating and PWM generation circuitry is shown on Page 39.

One of the A.G.C. rectifier outputs is fed to the R1/R2/C1 network. This provides the UK/EBU-standard 10ms integration response of the Model 255 A.G.C. circuit. The integrated peak signal is presented to one input of DC comparator IC1B. The other input monitors the A.G.C. control voltage. A difference between the integrated peak value of the program signal and the DC control voltage will cause IC1B to toggle; either to the negative supply if the program level is higher, or to the positive supply if the program level is lower.

IC1A is a very slow, inverting, integrating amplifier. For a fixed current through R6, the integrator will exhibit a segmented, dual time constant. When CR2 becomes back-biased, C3 is removed from a parallel-connection with C2, and the integration slope increases in rate. Thi develops an approximation of a constant-dB-per-unit-time for A.G.C. correction. R4 manually varies the A.G.C. RATE by setting the input current to IC1A.

A "0dB" DC voltage level is set by R10 and R11. IC2B compares this with the A.G.C. control voltage. During initial power-up, in the "PROOF" mode, or when the A.G.C. is otherwise defeated, a large error current through R7 rapidly returns A.G.C. GAIN to 0dB and holds it there. In normal operation, whenever the GATE "closes," a lower value of current is delivered to the integrator through IC5B. This causes the A.G.C. GAIN to very slowly seek the 0dB "resting" point.

The PWM-generation comparator for the A.G.C. function is identical to that for TRIBAND DRIVE. Comparator operation is detailed on Page 23.

Gating Circuitry

The secondary A.G.C. rectifier output is fed to IC4, a hysteresis comparator with a "syllabic" response to program material. The other comparator input is connected to voltage divider R41/R42. The A.G.C. control voltage at this point represents a -25dB level referred to "corrected" program "zero." Weighted program energy above the -25dB figure will "open" the GATE. This turns on IC5C to enable A.G.C., turns off IC5B to disable the "0dB-seek" function, and provides gating logic to the triband "floating platform" circuitry. The GATE is inhibited in "PROOF."

Triband Gain Control

The 3-band frequency-division, gain control and rectifier circuitry is shown on Page 37.

The leveled and preemphasized program audio is fed to the inputs of three inverting stages, IC8, IC9 and IC10. A capacitor around IC8 gives this stage a lowpass response, with a -3dB point at about 200Hz. Similarly, a capacitor around IC9 rolls this stage off at either 2120Hz or 3180Hz, depending on whether the 75- or the 50-microsecond characteristic capacitor is jumpered-in.

A portion of the 200Hz lowpass signal from IC8 is also fed to the input of IC9. Because IC8 is an inverting amplifier, the 200Hz lowpass characteristic is <u>subtracted</u> from the response of IC9. This yields a 200Hz - 2120Hz (or 3180Hz) <u>bandpass</u> response. Next, the lowpass <u>and</u> the bandpass signals are subtracted from the "flat" stage, IC10, which then assumes a <u>highpass</u> characteristic. In this manner, three separate, phase-coherent frequency bands are created. They will always recombine for an overall flat response, assuming that the three signal levels remain equal. The triband audio signals are, however, routed through PWM-driven CMOS switches to vary the gain in each band.

The output signal from each band in both the LEFT and the RIGHT channels is independently peak-rectified by a "precision" circuit consisting of two op-amp sections with diodes in the feedback path to compensate for rectifier diode forward drop. An equalization network ahead of the MID band rectifier corrects for a small (1.5dB) error which would otherwise occur during signal recombination under heavy gain reduction.

In each of the three bands, LEFT and RIGHT channel rectifier outputs are so summed that the common output represents the <u>highest</u> peak value of <u>either</u> the LEFT <u>or</u> the RIGHT channel. In addition, the MID band rectifier circuit has two independent, peak-responding outputs; one is used for normal gain control of MID channel energy, the other is integrated to derive a variable "platform" level for all bands.

MID Band Dynamic Reduction and "Platform" Circuits

Triband attack, release and "platform" timing and control circuits appear on Page 40.

Assuming the CMOS switch IC10D to be closed, the instantaneous peak value of rectified MID band program energy is held by the parallel combination of capacitors C19 and C18. The DC peak value passes through normally-closed IC11C to buffer stage IC9A, and directly to the MID band PWM-generation comparator, Q11, Q12 and Q13. As discussed in the "tutorial" on PWM at the beginning of this Section, the duty-cycle of the PWM is governed by feedforward techniques to maintain the output signal at a constant level. Operation of the five identical, discrete-component comparators is explained on Page 23.

The peak-rectified output from the second MID band control channel rectifier is integrated by R75 and C17 to form the basis of the "floating platform" program average level value. This is buffered by IC9B, and may be added to the program peak level value at a level somewhat lower than that of the peak. This is adjusted with the PLATFORM RATIO control, R77.

The average value of the "composite" MID band DC control signal (IC9A output) is recovered by the R86/C20 integrating network. This "platform" level, buffered by IC12B, governs the various processing release characteristics.

A fixed DC voltage corresponding to -6dB G/R is formed at the junction of R83 and R85. When the GATE closes, IC11D opens and MID band G/R is brought very slowly to its "resting" point through R84.

IC11A is closed whenever the GATE is open. This means that the MID band peak reduction value held by C19 and C18, and the initial platform value integrated by C17, can release (discharge) toward ground at rates determined by the MIDBAND DENSITY and PLATFORM RELEASE controls, R81 and R74, respectively. At the same time, the LF and HF SPECTRAL "LOADING" controls, R87 and R88, may be varied between the full platform value, and a value which is 6dB lower. This will dictate release in the other two bands.

When the GATE closes and IC11A opens, the two MID band release paths and the HF/LF "LOADING" levels each assume the full platform value. Gain in all three bands then releases to the platform level, holding there until the GATE again opens, or until gain eventually seeks its -6dB "resting" point.

HIGH Band D/R and Program-Adaptive Clipping

Peak-rectified HIGH band program signals charge C21 through IC10A. IC10C, normally closed, routes this peak DC level through buffer stage IC13A to the HIGH band PWM-generation comparator, Q14, Q15 and Q16.

The HIGH band G/R function has a complex, multiple release (C21 discharge) path. High frequency peak reduction in excess of the "floating platform" value releases through R97 and CR17 to the platform. As the HF SPECTRAL "LOADING" control is advanced, a correspondingly lower DC release level is available through R96. This not only increases the HIGH band release rate, but the final release level falls below that of the MID band platform. Thus the HF "LOADING" control permits the user to simultaneously increase the average level within the HIGH band, and the average level of the HIGH band with respect to that of the MID band. Effects of HF "LOADING" are further discussed on Page 7.

C23 and R103 generate a first derivitive of the peak-derived HIGH band control signal. The AC level presented to IC14B represents "activity" in the HIGH band. This circuit, the "High Frequency Activity Detector" (H.F.A.D.) is associated with the Program-Adaptive Clipping function.

CR26 establishes the H.F.A.D. threshold. Whenever high frequency activity exceeds this value, the output of IC14B toggles to the positive rail. This charges C24, sending the output of IC14A negative for the duration of C24's discharge through R104. When the output of IC14A goes negative, IC10A and IC10D switch from a normally-closed to an open state.

In the MID band channel, C18 is switched out of a direct parallel connection with C19. R79, now in series with C18, establishes a dual attack/release characteristic. This causes more clipping-like action for very fast MID band program peaks, but still within control of the feedforward G/R function. In the HIGH band, IC10A removes C21 from the circuit entirely, and the HIGH band G/R function reverts entirely to feedforward clipping.

The threshold and time constants of the H.F.A.D. are selected to restrict Program-Adaptive Clipping to only those instances where there is sufficient high frequency activity to mask audible effects.

LOW Band Dynamic Reduction

Peak-rectified LOW band energy charges C25. The peak value is buffered by IC12A and feeds the LOW band PWM-generator comparator, Q17, Q18 and Q19. When the LF SPECTRAL "LOADING" control is fully CCW (0dB), C25 discharges through R92 to the "floating platform" value. As the "LOADING" control is advanced, C25 discharges to a point lower than the platform. This both shortens the release time, increasing "density" in the LOW band, and lowers the final release value toward 0dB, increasing the average level of the LOW band with respect to the MID.

The three CMOS switches, IC11C, IC10C and IC10B, are normally closed to pass peak-rectified program signals to the control circuitry. These open in the "PROOF" mode to inhibit Dynamic Reduction circuit operation.

Triband Combiner, Clipper and Output Stages

IC19 (Page 38) is an active, lowpass combining stage for the PWM-controlled LOW, MID and HIGH band program signals. The two complementary transistor pairs, Q1/Q2 and Q3/Q4, are active, "safety" clippers for LEFT and RIGHT program audio. The transistor clippers are biased just above the PWM-limited peak excursions, and act only on peaks which exceed limiter attack time.

Despite the lowpass characteristic of the combining amplifier, IC19, the output signal still contains components of the PWM waveform. Because the active clipping stages are within the feedback loop of IC19, clipping action does not conform to the expected characteristic but, rather, to a more subtle one with a far less harsh result.

IC20 is both a deemphasis stage and the output amplifier for one phase of the output signal. It may be jumpered to conform to either the 75- or 50-microsecond curve, or to a "flat" response with a two-pole lowpass function above 20kHz. IC21 is the unity-gain inverter which supplies the output signal of opposite phase. 300-ohm buildout resistors give the active-balanced line output a 600-ohm, resistive source impedance.

G/R Indicator Circuitry

Scaling for the A.G.C. and the Dynamic Reduction G/R readouts is linear-dB; 3dB/step for A.G.C., 2dB/step for D/R. Because readily-available, linear-voltage LED bargraph driver ICs are used, scaling conversion circuitry is required.

Referring to Page 39, IC6 is the amplifier which converts the linear-voltage, A.G.C. G/R control signal to the linear-dB function for the display.

IC6B is a simple inverting stage with a "segmented" feedback network. R29 sets the initial gain of the stage. As the positive DC control input voltage rises, the output of IC6B begins to go negative. When the output brings the junction of R30 and R31 to -0.6V, CR6 is biased "on," and R31 parallels R29 in the feedback path. R33 and R35 are similarly brought into the circuit at different bias points. The net effect is a 4-slope "compound" of the desired transfer function. Because diode turn-on is not abrupt, the function is a better approximation of the required smooth curve than segmentation might suggest.

The output voltage range of IC6B is 0 to -10VDC for the nominal A.G.C. working range. This is translated to a +10 to 0VDC range by IC6A, a unity-gain "offset" amplifier. Thus as input DC control voltage increases (reducing A.G.C. gain) a voltage is delivered to the LED driver which drops from a nominal +10 volts toward ground.

Similar scaling conversion circuits are required for each of the triband G/R indicators. These appear on Page 40.

Three identical converters serve the MID, HIGH and LOW bands. These are IC15, IC16 and IC17, respectively. IC13B, which feeds the HIGH band converter, performs a peak-holding function to make Dynamic Reduction visible on the display despite the very fast HIGH band attack and release.

Using MID band circuitry as an example, initial gain of IC15B is established by R107 and R108. Positive-going MID band DC control voltage drives the output of IC15B negative. When the junction of R109 and R110 reaches -0.6V, CR28 turns on to switch R110 in parallel with R108, changing gain. As the output is driven even more negative, the junction of R111 and R112 eventually reaches the turn-on of CR29, and R112 is switched into the feedback path also. This creates the 3-slope, segmented transfer function required for linear-dB display of MID band Dynamic Reduction.

IC15A translates a 0 to -10V range at the output of IC15B to a +10 to 0V drive to the display board.

The four LED-driver ICs and associated LED "strings" are shown in the Display Board Schematic at the bottom of Page 41.

Each of the four LED drivers contains a series of internal comparators. These turn on the LEDs in the readout string in direct, linear response to the input voltage. A +8V reference is supplied to all four ICs and feeds the "top" of an internal voltage divider, also monitored by the comparators. This reference sets the transition point between the "top" LED in the string and the next.

Power Supply

The dual, bipolar power supplies are diagrammed at the top of Page 41.

A dual-primary power transformer accommodates both 115V and 230V (nominal) AC mains voltages. The primary voltage is selected with the jumpering strip described on Page 11.

"Raw" DC supplies are first regulated to positive and negative 15 volts by IC19 and IC20, and to bipolar 6 volts by IC21 and IC22. The four regulators are the "3-terminal, adjustable" type, with output voltage set by a divider between the regulated output and an internal reference.

IC23 buffers a resistive divider to create the +10V and +8V reference supplies for the display circuitry.

V APPENDIX

(Parts Lists - Schematics - Warranty)

PARTS LIST - INOVONICS MODEL 255

("TRIBAND / PWM" PROCESSOR)

- - - - - ANALOG BOARD - - - - -

SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)
Capacitors		
C1,2,18,19	0810	DM-15 Mica; 100pF, 5%, 600V (open)
C3,4,17,20,21, 34,49,53,58	1052	Electrolytic; 22uF, 25VDC (open, radial)
C5,6,22,23,36, 38,40,45,54, 55,63,64	0884	Polycarbonate; .001uF, 5%, 100V (WIMA / FKC-2)
C7,24,53,62	0814	DM-15 Mica; 220pF, 5%, 600V (open)
C8,25	0808	DM-15 Mica; 68pF, 5%, 600V (open)
C9,10,14,26, 27,31,50,59	0876	Polycarbonate; 470pF, 5%, 100V (WIMA / FKC-2)
C11,28	0931	Polyester; .022uF, 5%, 63V (WIMA / MKS-2)
C12,29,57,66	0895	Polyester; .033uF, 5%, 63V (WIMA / MKS-2)
C13,30	1083	Polycarbonate; .0047uF, 5%, 100V (WIMA / FKC-2)
C15,16,32,33, 51,52,56,60, 61,65	1081	Polycarbonate; .0022uF, 5%, 100V (WIMA / FKC-2)
C35,37	0932	Polyester; .1uF, 5%, 63V (WIMA / MKS-2)
C39,42,43,44, 47,48,63,64	0930	Polyester; .01uF, 5%, 100V (WIMA / MKS-2)
C41,46	1080	Polycarbonate; .0015uF, 5%, 100V (WIMA / FKC-2)
C57,66	1086	Polypropylene; .0033uF, 2.5%, 100V (WIMA / FKP-2)
C67-72	1053	Tantalum; 2.2uF, 25V (open, radial)
Diodes		
CR1-40	1100	Silicon signal; 1N4151 (open)
Integrated Circuits		
IC1,2,4,5,8, 9,10,19	1375	FET-Input Dual Op-Amp; LF353N (open)
IC3,11,12	1335	CMOS Quad Analog Switch; CD4066BE (open)
IC6,7,13,14, 15,16,17,18	1313	Dual Op-Amp; RC4558NB (RAYTHEON, T.I.)
IC20,21	1314	Dual Op-Amp; NE5535N (SIGNETICS)

PARTS LIST - Analog Board (continued)

SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)

Transistors

Q1,3	1205	PNP, Gen. Purp.; 2N3906 (open)
Q2,4	1204	NPN, Gen. Purp.; 2N3904 (open)

Resistors

UNLESS NOTED BELOW, fixed resistor values are per schematic notation, in ohms (K = X1000, M = X1Meg). With no tolerance specified, resistor is 5%, 1/4-watt carbon film; 1% resistors are 1/4-watt, metal film.

R11,35	0508	Multiturn Trimmer; 2K (BECKMAN / 89PR2K)
R113,124	0511	Multiturn Trimmer; 20K (BECKMAN / 89PR20K)

Miscellaneous

S1	1857	Switch, DPDT Miniature Slide, Side-Actuated (CW INDUS. / GI-152 PC)
- -	1737	0.1-inch-spacing "Shunt" (Jumper for Option Selection)

- - - - - CONTROL BOARD - - - - -

SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)

Capacitors

C1,5,6,11, 12,16,21	0932	Polyester; .1uF, 5%, 63V (WIMA / MKS-2)
C2,13,14,15, 17,20,26,27, 30-34	1053	Tantalum; 2.2uF, 25V (open, radial)
C3	1054	Tantalum; 4.7uF, 25V (open, radial)
C4,22,24,25	1059	Polyester; .47uF, 5%, 63V (WIMA / MKS-2)
C7,9	0810	DM-15 Mica; 100pF, 5%, 600V (open)
C8	0806	DM-15 Mica; 47pF, 5%, 600V (open)
C10	0818	DM-19 Mica; 470pF, 5%, 600V (open)

PARTS LIST - Control Board (continued)

SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)
C18	1087	Polyester; .22uF, 5%, 63V (WIMA / MKS-2)
C19,23	0930	Polyester; .01uF, 5%, 63V (WIMA / MKS-2)
C28,29	0902	Electrolytic; 1000uF, 35V (open, axial)

<u>Diodes</u>

CR1-33	1100	Silicon Signal; 1N4151 (open)
CR34-41	1125	Silicon Rectifier; 1N4005 (open)

<u>Integrated Circuits</u>

IC1,9,12,13	1375	FET-Input Op-Amp; LF353N (open)
IC2,3,4,6,14, 15,16,17,23	1313	Dual Op-Amp; RC4558NB (RAYTHEON, T.I.)
IC5,10,11	1335	CMOS Quad Analog Switch CD4066BE (open)
IC7	1336	CMOS Hex Inverter; CD4069BE (open)
IC8,18	1342	CMOS Quad AND; CD4081BE (open)
IC19,21	1373	Pos. Volt. Reg.; LM317T (open)
IC20,22	1374	Neg. Volt. Reg.; LM337T (open)

<u>Transistors</u>

Q1,2,3,7,10, 13,16,19	1205	PNP, Gen. Purp.; 2N3906 (open)
Q4	1204	NPN, Gen. Purp.; 2N3904 (open)
Q5,6,8,9,11, 12,14,15, 17,18	1210	NPN, High Beta; 2N5088 (open)

<u>Resistors</u>

UNLESS NOTED BELOW, fixed resistor values are per schematic notation, in ohms (K = X1000, M = X1Meg). With no tolerance specified, resistor is 5%, 1/4-watt carbon film; 1% resistors are 1/4-watt, metal film.

R4,66,77, 87,88	0573	Sgl. Turn Trimmer; 10K (CTS / X201R103B)
R48	0557	Sgl. Turn Trimmer; 2K (BECKMAN / 91AR2K)
R74,87	0574	Sgl. Turn Trimmer; 1 Meg (CTS / X201R105B)

PARTS LIST - Control Board (continued)

SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)
Miscellaneous		
I1	2022	LED, Clear/Red, T1 (STANLEY / SBR 3901)
T1	1523	Power Transformer, Dual Primary, PC-mounting (TRIAD / FP34-340, SIGNAL / LP-34-340)
- -	1737	0.1-inch-spacing "Shunt" (Jumper to Select Options)
- -	1723	8-position Female "Shell" for Mains Voltage Selection Jumper
- -	1674	Terminals to fit "Shell," above; 4 required.
- -	2605	Silicone Rubber Mounting Washer for TO-220 Voltage Regulators
- -	2604	Fiber Shoulder Washers for mounting TO-220 Voltage Regulators

- - - - - DISPLAY BOARD - - - - -

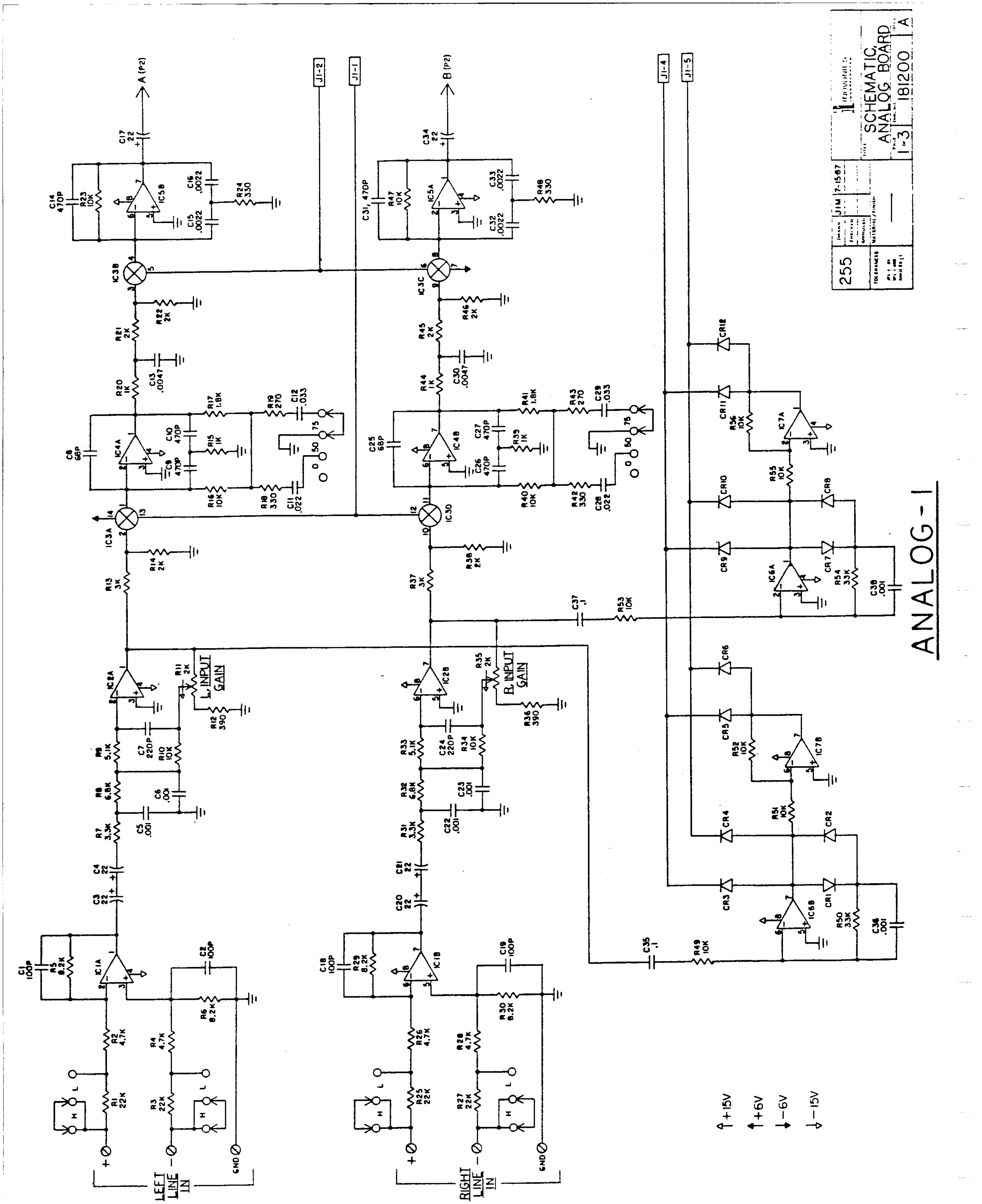
SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)
Capacitors		
C1,2	1053	Tantalum; 2,2uF, 25V (open, radial)
Diodes		
CR1	1100	Silicon Signal; 1N4151 (open)
Indicators		
I1-40	2019	LED, Red/Red, T1-3/4 (STANLEY / SPR 5731)
Integrated Circuits		
IC1-4	1376	Display Driver; LM3914N (NAT'L)

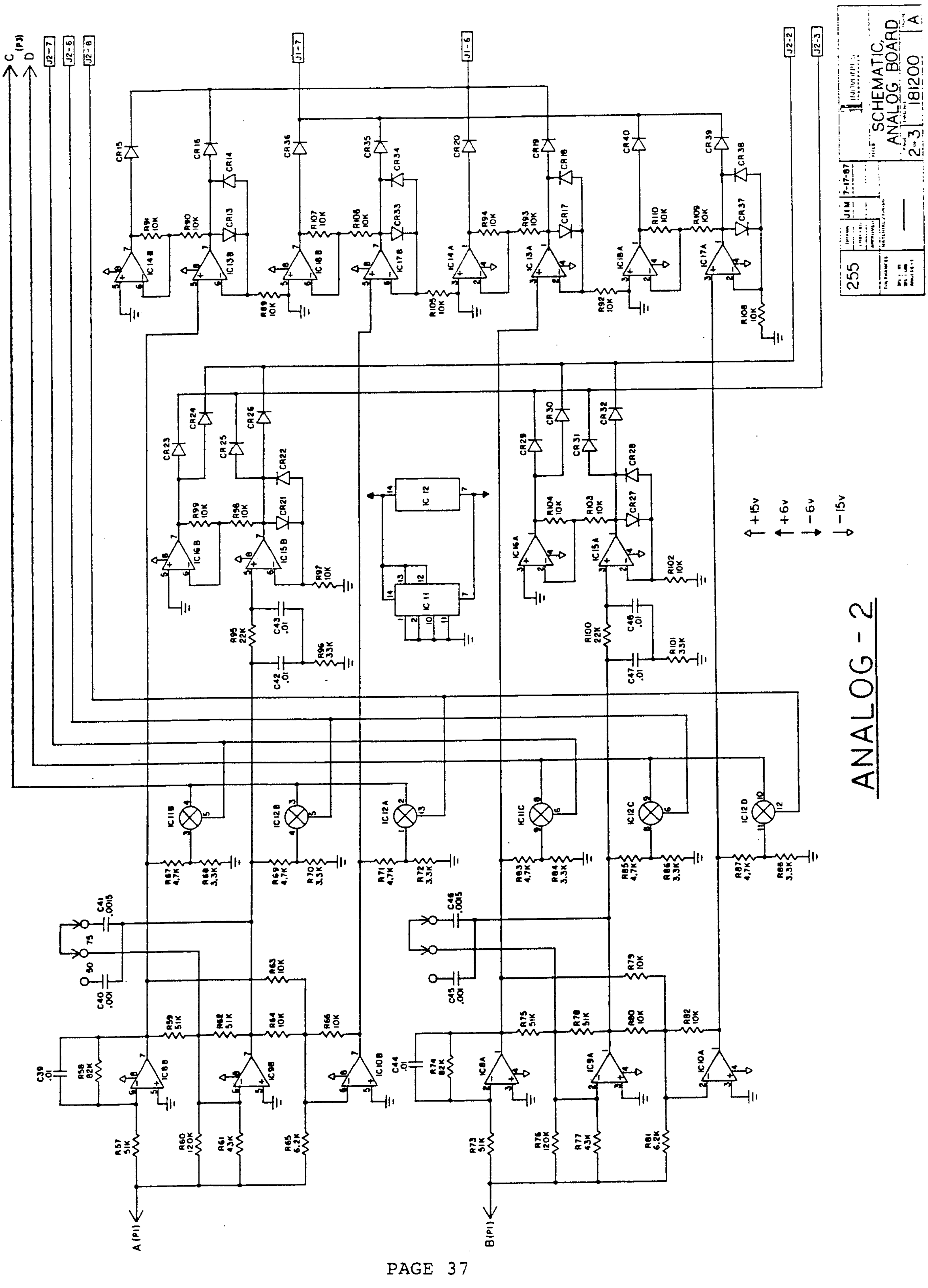
PARTS LIST (continued)

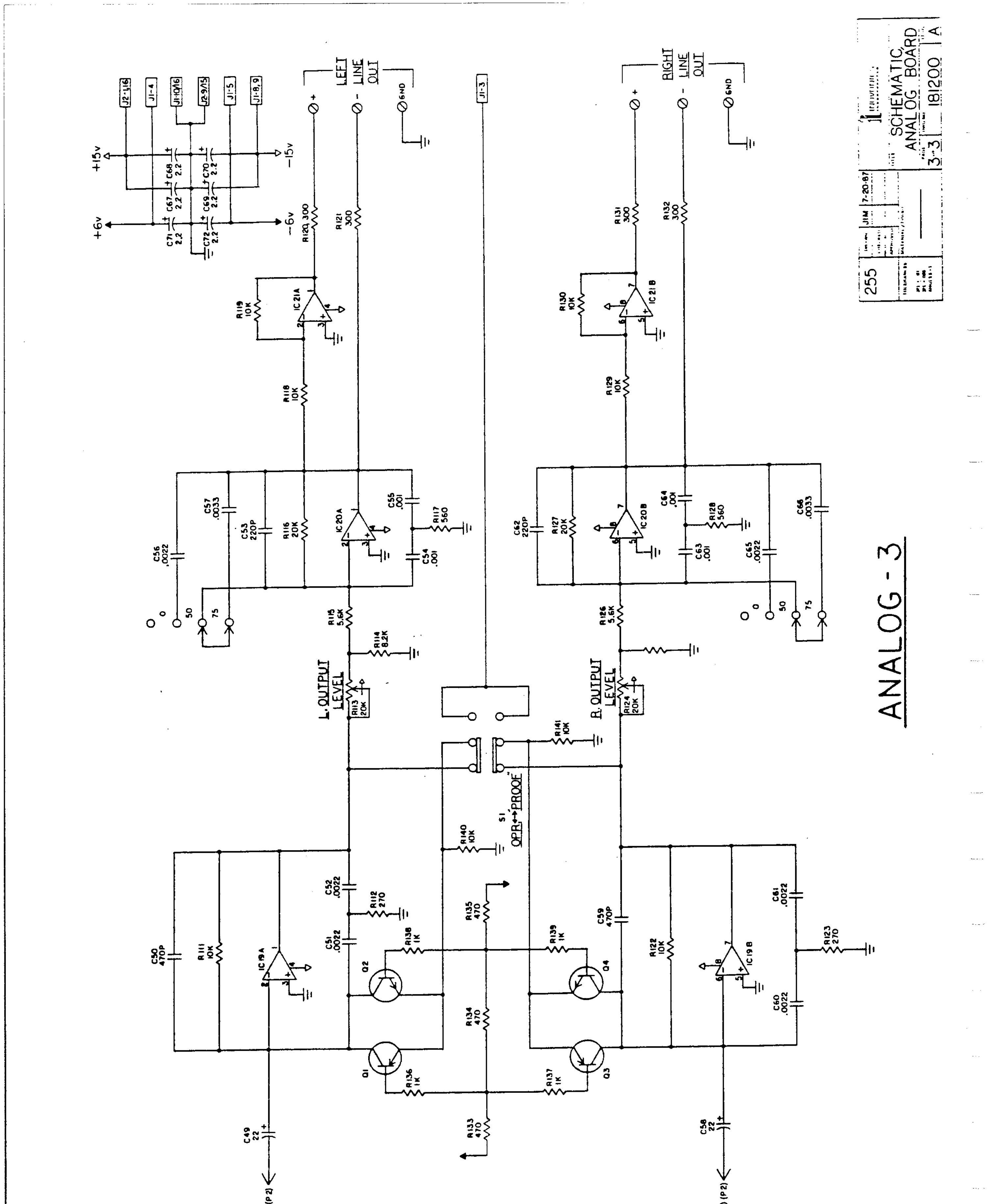
SCHEMATIC DESIGNATION	INOVONICS PART NO.	COMPONENT DESCRIPTION (MFGR. / MFGR. P/N)

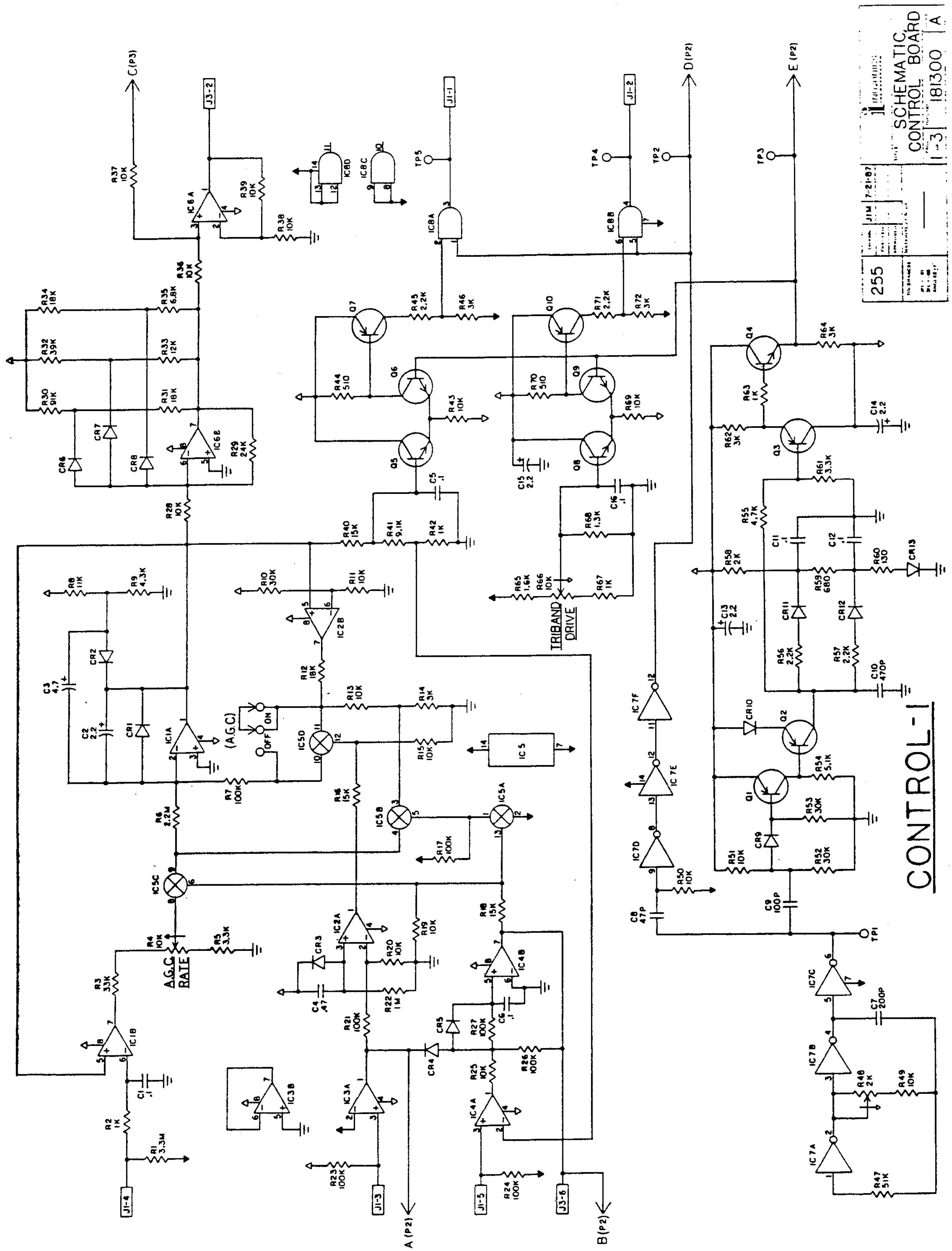
Chassis Parts

C1,2	1064	Capacitor, Disc Ceramic; .005uF, 1kV (open)
S1	1816	Power Switch; SPDT Slide (CW INDUS. / GF-324)
- -	1666	Connector, Male, 16-pin DIP; as required for ribbon cables (AMPHENOL "SPECTRA-STRIP" / 842-815-1601-134)
- -	2942	Ribbon Cable, 16-conductor; as req'd (AMPHENOL "SPECTRA-STRIP" / 191-2801-016)

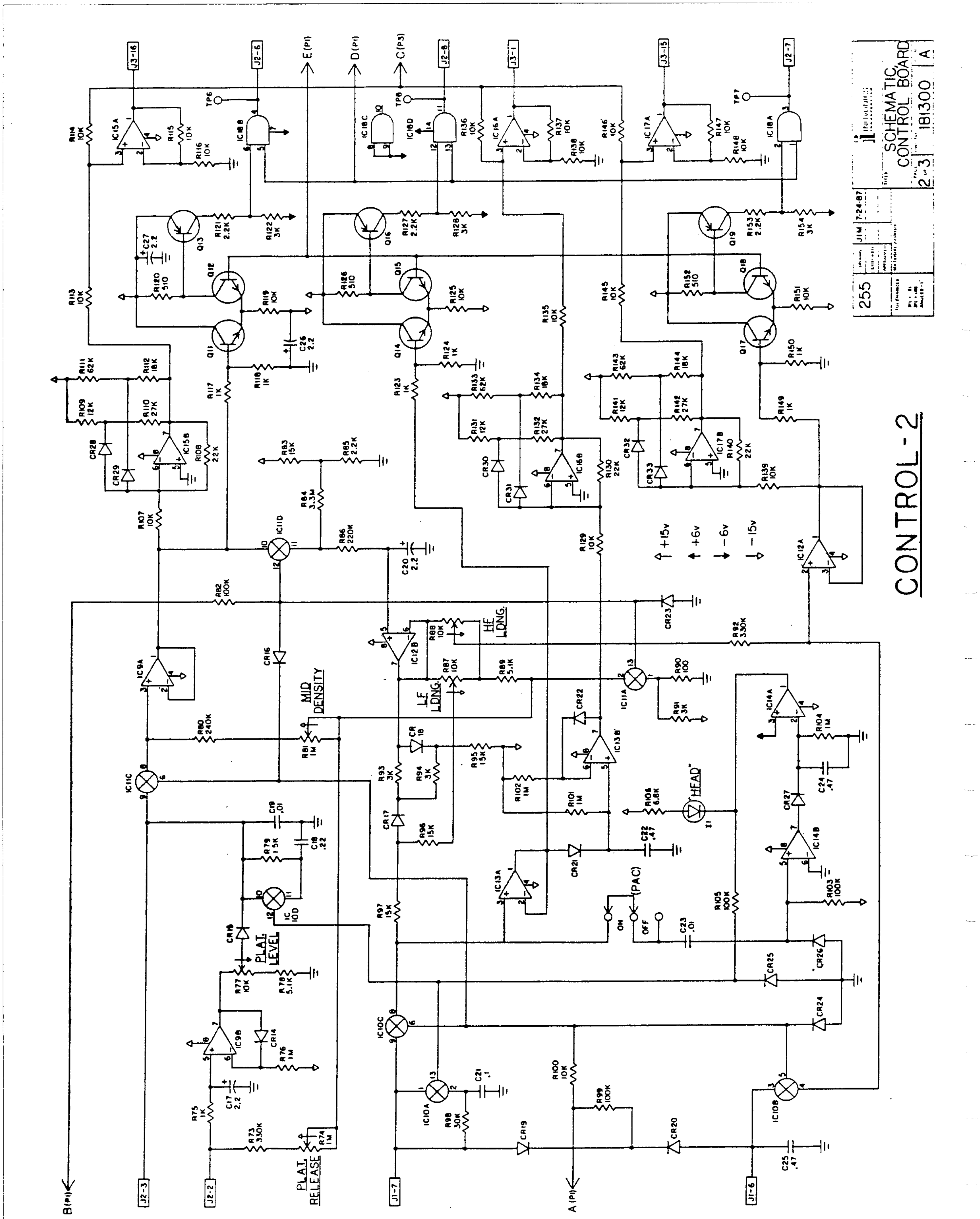

SCHEMATIC, ANALOG BOARD
181200
255
ANALOG-1
LEFT LINE IN
RIGHT LINE IN
L. INPUT GAIN
R. INPUT GAIN
+15V
+6V
-6V
-15V

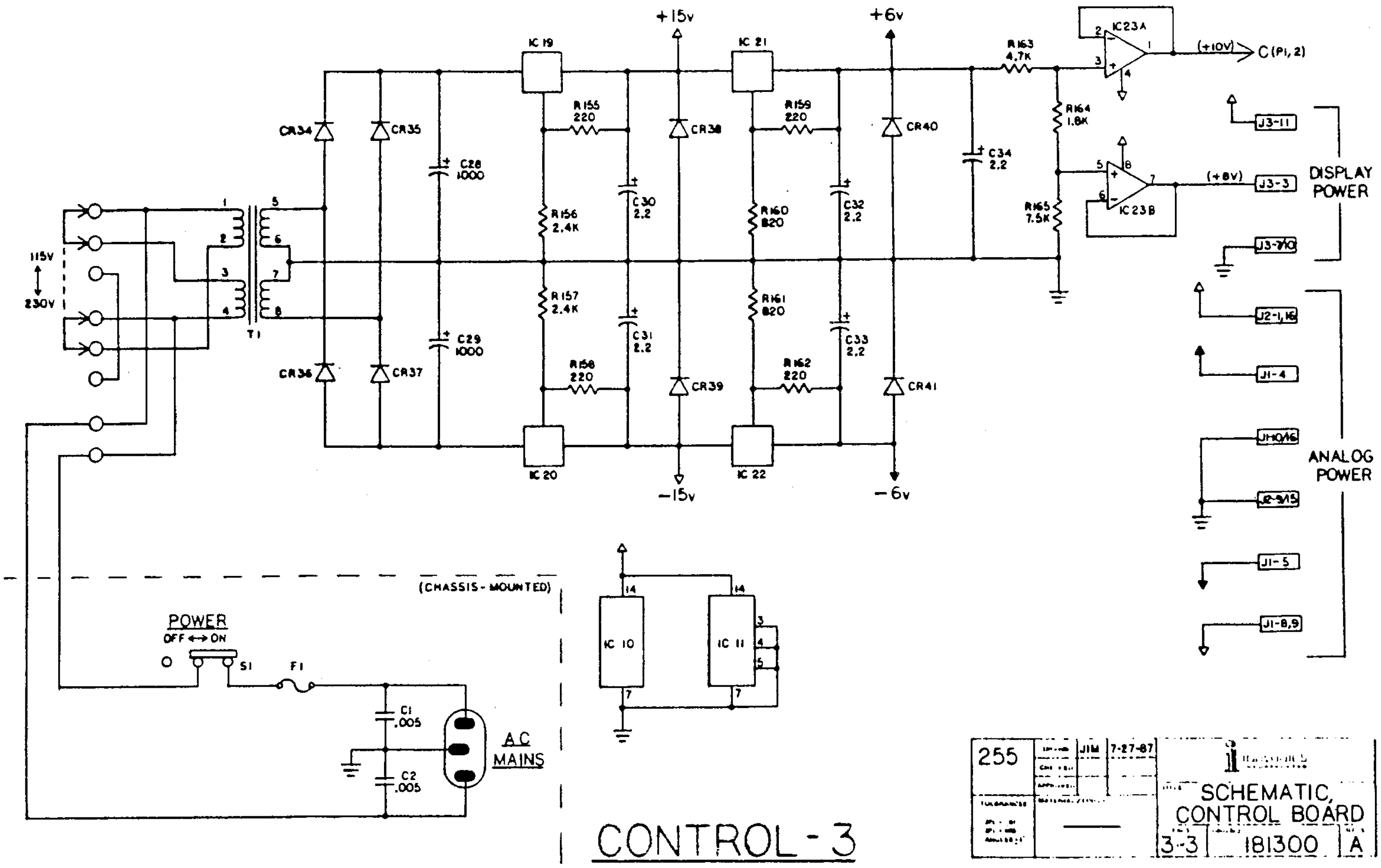

ANALOG - 2
SCHEMATIC, ANALOG BOARD
181200
255
JIM 7-17-87
2 of 3
A
A (P1)
B (P1)
C (P3)
D
J2-7
J2-6
J2-8
J1-7
J1-6
J2-2
J2-3
+15v
+6v
-6v
-15v


ANALOG - 3
SCHEMATIC, ANALOG BOARD
255
181200
3-3
A
7-20-87
LEFT LINE OUT
RIGHT LINE OUT
L. OUTPUT LEVEL
R. OUTPUT LEVEL
S1 OPR↔PROOF
C (P2)
D (P2)
+15v
-15v
+6v
-6v

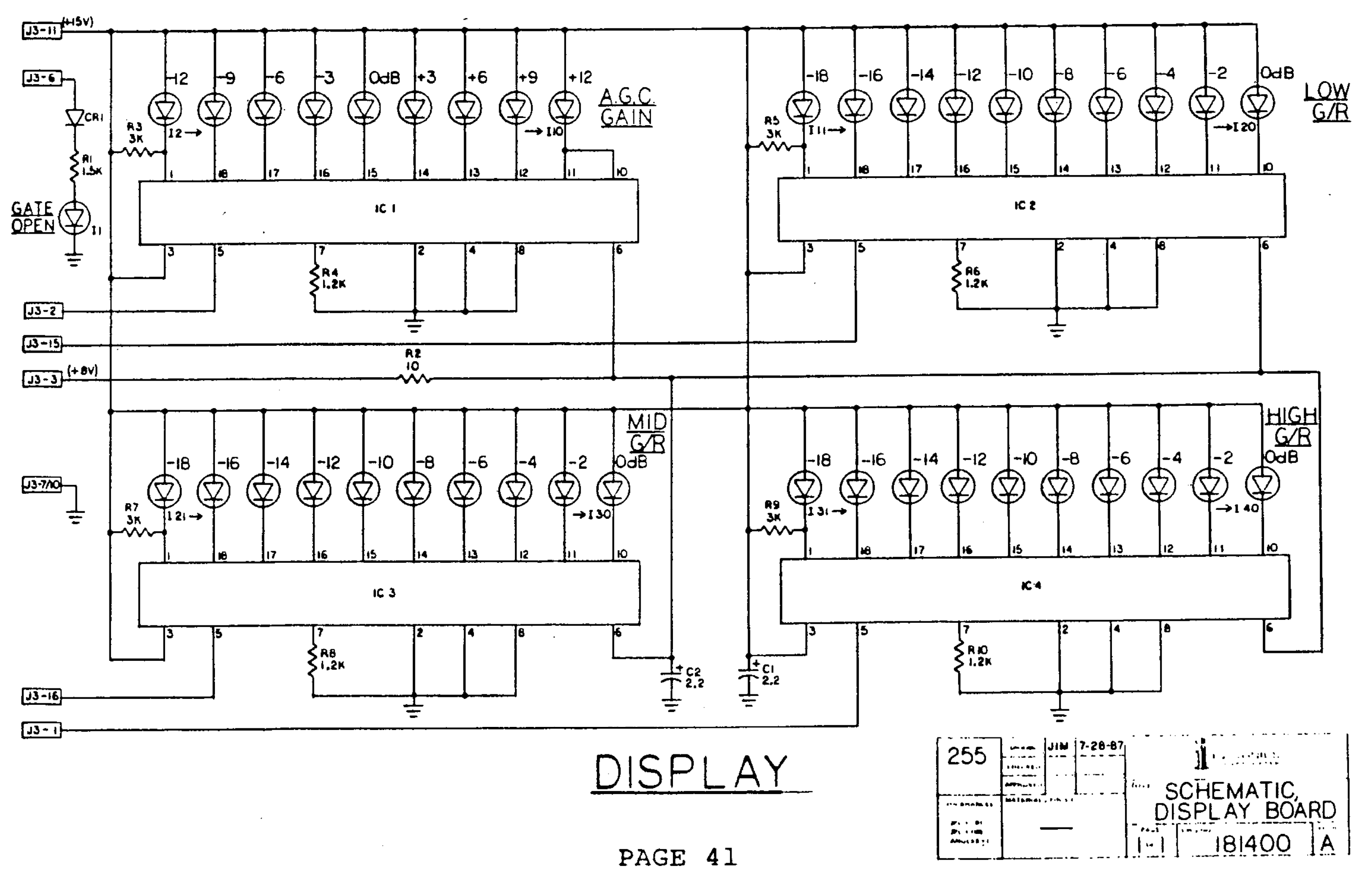


SCHEMATIC, CONTROL BOARD
181300
A
255
7-21-87
CONTROL-I
TRIBAND DRIVE
A.G.C RATE
(A.G.C)


CONTROL-2
SCHEMATIC, CONTROL BOARD
IB1300
A
255
2 of 3
7-24-87
MID DENSITY
PLAT LEVEL
PLAT RELEASE
HF LDNG.
LF LDNG.
"HEAD"
(PAC)
ON
OFF
+15v
+6v
-6v
-15v
B(P1)
A(P1)
E(P1)
D(P1)
C(P3)
J2-3
J2-2
J1-7
J1-6
J3-16
J2-6
J2-8
J3-1
J3-15
J2-7
TP6
TP8
TP7



+15v
+6v
-15v
-6v
115V
230V
DISPLAY POWER
ANALOG POWER
(CHASSIS-MOUNTED)
POWER
OFF ↔ ON
AC MAINS
CONTROL - 3
255
JIM 7-27-87
SCHEMATIC, CONTROL BOARD
3-3
181300
A



A.G.C. GAIN
LOW G/R
MID G/R
HIGH G/R
GATE OPEN
DISPLAY
255
JIM 7-28-87
SCHEMATIC, DISPLAY BOARD
1-1
181400
A

INOVONICS WARRANTY

Inovonics, Inc. products are warranted to be free from defects in material and workmanship. Any discrepancies noted within 90 days of the date of purchase will be repaired free of charge. Additionally, parts for repairs required between 90 days and one year from the date of purchase will be supplied free of charge, with installation billed at normal rates. It will be the responsibility of the purchaser to return equipment for warranty service to the dealer from whom it was originally purchased unless prior arrangement is made with the dealer to inspect or repair at the user's location.

This warranty is subject to the following conditions:

1. Warranty card supplied with the equipment must be completed and returned to the factory within 10 days of purchase.

2. Warranty is void if unauthorized attempts at repair or modification have been made, or if serial identification has been defaced, removed, or altered.

3. Warranty does not apply to damage caused by misuse, abuse, or accident.

4. Warranty valid only to original purchaser.

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