OPERATING & MAINTENANCE INSTRUCTION MANUAL

MODEL 250

PROGRAMMABLE PROCESSOR

USER'S RECORD

Model 250 - Serial No. _____

Date Purchased _____

Warranty Card Sent ☐

Purchased From _____

INSTRUCTION MANUAL

MODEL 250

PROGRAMMABLE AUDIO PROCESSOR

July, 1983

(Revised June, 1994)

INOVONICS
INCORPORATED

1305 Fair Avenue – Santa Cruz, CA 95060

Tel: 831-458-0552 Fax: 831-458-0554

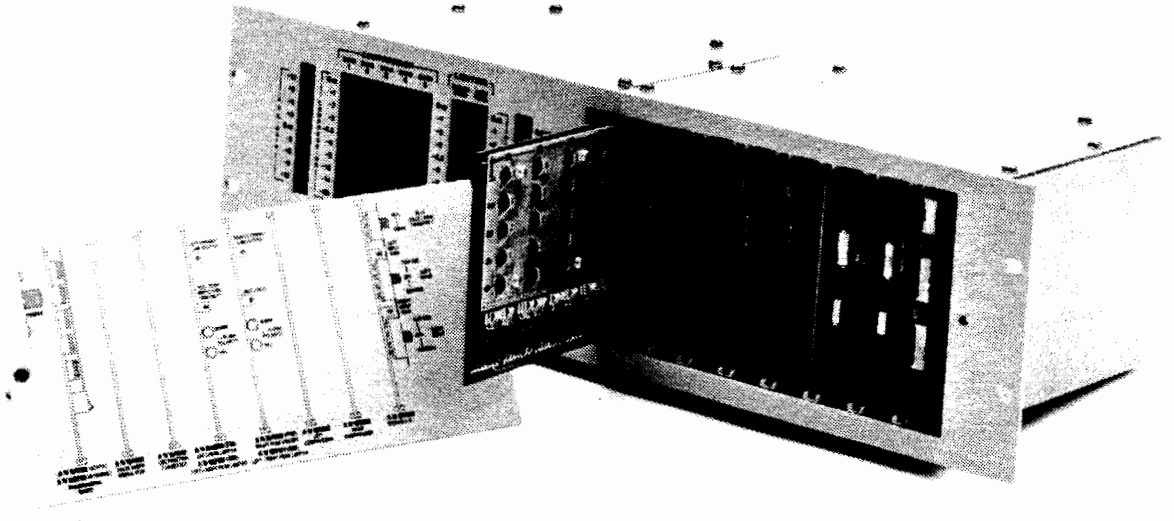
TABLE OF CONTENTS

I GENERAL DESCRIPTION

The Inovonics 250 is a parameter-programmable stereo broadcast audio processor intended as the only signal conditioner required between the broadcast console and the transmitter.

Available in either of two versions, the 250-00 serves in FM-stereo, TV-aural and certain audio production and recording applications. The 250-01 is specifically for AM-stereo (or mono) use.

The unique feature of the Inovonics 250 is its programmability. Many of the processing parameters, particularly the subjective ones, may be pre-programmed for variable station formats, changing audience profiles or to accommodate special program input signal situations. The processing presets may then be selected as appropriate to address a particular need. Alternately, an accessory circuit assembly can replace the manual programming function with a computer interface option for continuous, on-line computer control of the processing system.



II FUNCTIONAL DESCRIPTION AND SPECIFICATIONS

The Inovonics 250 falls under the product classification of a "Multi-Function, Multiband Audio Processor." It combines slow, gain-riding A.G.C., multiband compression, graphic equalization and a choice of final peak limiters; one specifically for FM and TV, one for AM-stereo. Each of the functional elements will be discussed separately, as will the relation of each to the aspect of processor programmability. Performance specifications not expressed or implied in the discussions or accompanying illustrations are tabulated at the end of this section.

Traditionally, an audio processor, especially a multiband unit, has had primary application in maximizing broadcast carrier modulation and program density. Processor designs have addressed the broadcasters' desire to be "LOUD." The "louder is better" school certainly still has its following, though format and good programming are invariably the keys to any station's success. With several stations in any one market providing nearly identical programming, however, long term listenability emerges as a real and critical factor in audience satisfaction and higher quarter-hours.

This manual is divided into sections to best present the features, design philosophies, installation and operation aspects of the Inovonics 250. Many of the specifications and operating instructions are expressed in the manual text, rather than in the more usual tabular form. Thus it is recommended that the manual be thoroughly digested prior to placing the unit in service.

The Inovonics 250 Block Diagram, Figure 1 on the following page, may be of help in connection with the discussions of the various Processor elements.

Automatic Gain Control (A.G.C.)

The output program mix from an audio console will invariably be subject to long-term level variations. One might naturally attribute these variations to inattention by the board operator, especially in a combo operation with duties more pressing than consciencious gain-riding. Another cause of level inequalities stems from the manner in which different operators respond to the level meter. These probably are the primary human elements

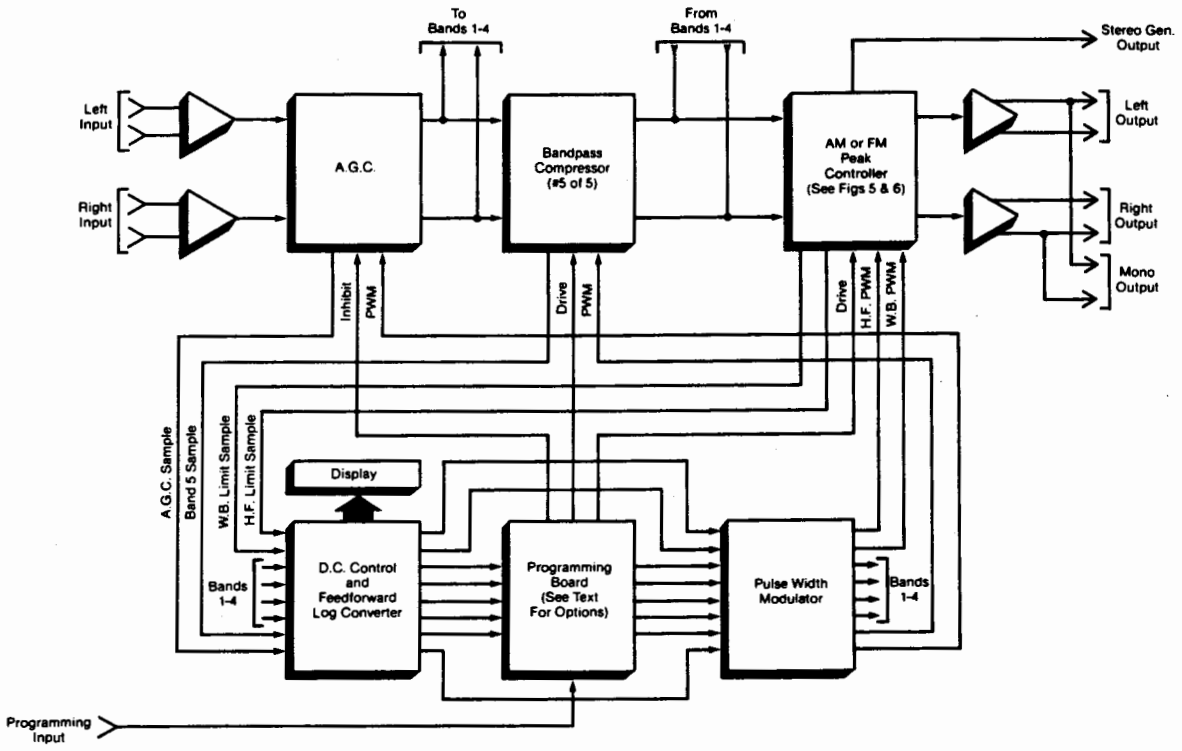


Figure 1 - Block Diagram

responsible for level variations.

The "VU" meter was developed for, and has been used in broadcasting for about fifty years. A number of factors have changed since the original specification was written for this device. Until fairly recently, audio entertainment consisted of speech and either recorded symphonic or "popular" music which, because of the state of audio science, had a restricted and predictable average-to-peak ratio. Contemporary music and recording techniques, on the other hand, can yield much higher average/peak ratios which are not accurately represented by the sluggish VU meter.

The European practice, and that of "enlightened" domestic recording and broadcasting facilities, is to establish audio levels based on the indication of a quasi-peak-responding "Peak Program Meter." The PPM provides a much more accurate display of program dynamics in terms of system headroom and overload margin. For this same reason, the slow A.G.C. stage of the Inovonics 250 employs the same 10-millisecond-integration peak response characteristic of the UK / EBU-standard PPM. The correction rate of

the A.G.C., on the other hand, is a very slow, unobtrusive 0.5dB-per-second. This slow input level correction approximates manual gain control and does not result in program level compression or other alteration of the program dynamics. It does, nevertheless, present the following processing stages with a constant, peak-weighted level.

To inhibit unnecessary "hunting" in the absence of program, the A.G.C. circuit is "gated." Gain is held at the previous value until the program returns. During extended signal loss, gain is slowly brought back to a 0dB, unity-value figure at a rate somewhat slower than that for level correction. The gating circuit is frequency-weighted to recognize only legitimate program material. This prevents the A.G.C. from reacting to background noise, such as a crowd at a ball game. The gating control channel samples L+R energy, with -3dB points at 300Hz and 3kHz. Threshold sensitivity is preset to open the gate when the L+R midband program energy exceeds -25dB relative to nominal, corrected program "zero" level.

Left and right A.G.C. gain are under common control to preserve stereo image. Gain is established by sampling both channels independently and reacting to the higher level.

There are instances in which it is desirable to inhibit A.G.C. action altogether. Classical music programming exemplifies a case in which the long-term program dynamics would want to be preserved. For this reason, the choice to use A.G.C. is a programmable Processor function. A.G.C. may be turned on or off for any of the processing presets.

To facilitate setup of the Inovonics 250, a sine wave tone generator is included as part of the A.G.C. circuit assembly. The generator may be switched between 500Hz and 5kHz, and can be applied to either the left, the right or to both Processor channels. The tone generator output is injected into the A.G.C. input circuit after the INPUT GAIN controls; these controls will have no effect on the tone generator signal.

Multiband Compression

To be unobtrusive in its operation, an audio level compressor must be fast acting; it must follow the program signal envelope closely. A fast attack is needed to reduce sudden level increases, and a fast recovery to prevent "holes" and audible fade-up when the input level returns to the previous, lower value.

Fast compressor action is not consistent with low distortion, however, particularly at lower frequencies. Short control channel time constants cause amplitude modulation of the program by

its own harmonic products, and intermodulation between different program frequency components. By dividing the spectrum into two or more bands of frequency-discriminant compression with longer time constants for the lower frequencies, the tradeoff between compression side-effects and signal distortion can be almost entirely eliminated.

Although a simple, two-band frequency-discriminant level compressor can be free from most unwanted processing side-effects, additional advantages can be gained by further frequency band division. Program "density" can be increased, for instance, and a greater number of frequency bands "squeeze" more energy into the audio spectrum. Moreover, if the static gain of each band is made manually variable, a form of graphic equalization can be afforded as well; again, the greater number of bands yielding the most comprehensive control.

There are, of course, practical and economic limits to frequency-discriminant compression, and very important audio quality considerations as well. With a greater number of bands and the attendant increase in program density, a "business" is imparted to the program which can lead to a "flat" sound and greater listener fatigue. Also, a greater number of frequency bands necessarily require steeper band filter skirts and severe response irregularities at the filter crossover points when gains differ in adjacent bands. The audible effect in this case is a "phasing" or "swishing" sound.

The Inovonics 250 employs five bands of frequency-discriminant compression. This is a quality-motivated compromise between the considerations of program density and subjective program quality degredation. The three center bands are each two octaves wide, and the bottom and top bands have high- and low-pass characteristics, respectively. All are first-order filters with very gentle 6dB-per-octave skirts. Filter amplitude response and overall combined response is graphed in Figure 2. Phase response of the combined filters is linear when band gains are at similar values.

Within each band, the filtered program frequency components undergo dynamic range compression with full left/right correlation to preserve stereo image. The compressors are of an open-loop, "feedforward" design with a program-controlled compression ratio which increases with input level. This characteristic is shown in Figure 3. The gentle transition of the signal from a linear to a compressed state permits a good deal more compression than usual before the program begins to sound heavily compressed.

The broadband input level to the multiband compressor is one of the programmable functions, and affords user control over program

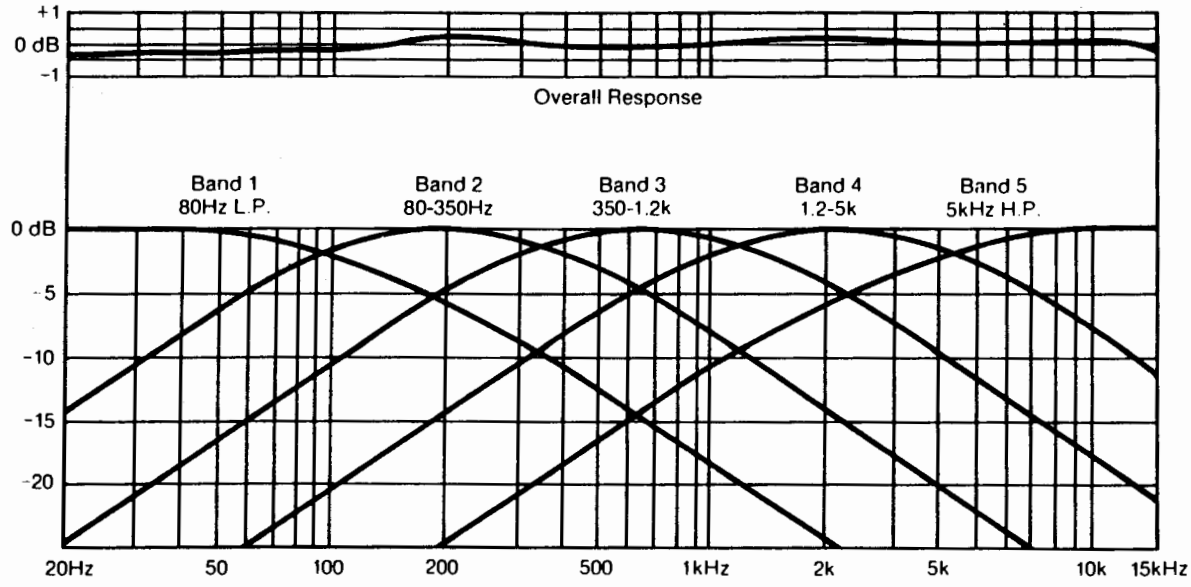


Figure 2 - Multiband Compressor Filter Response

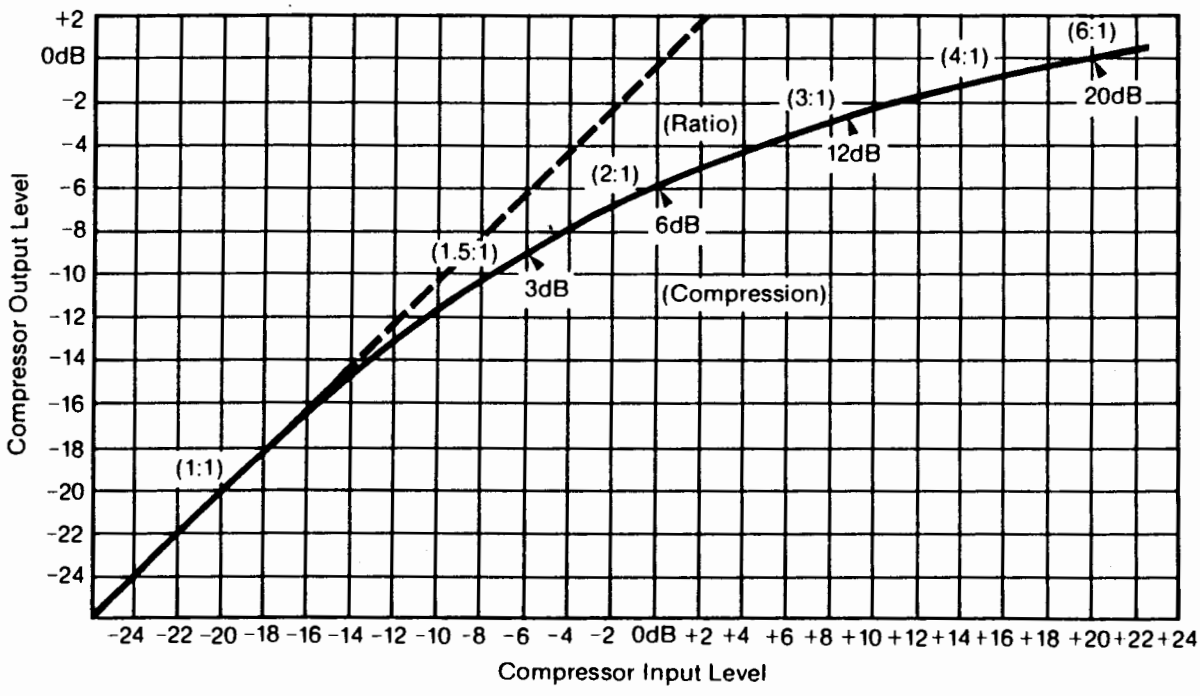


Figure 3 - Compressor Transfer Characteristic

density. Nominal compression may be preset at 3, 6, 9 or 12dB. With each input gain figure, overall compressor gain is normalized so that subsequent processing is not altered.

Attack and recovery timing for the five compression bands is fixed in the Inovonics 250, each optimized for the processed frequency band as the best compromise between rapid action and low signal distortion.

Graphic Equalization

The five bands of program compression are also used for equalization. The output level from each band is made externally (programmably) variable to afford frequency contouring of the recombined broadband program signal.

In order to give sufficient control over program equalization, yet lessen the chance for audio quality degredation through equalizer misuse, EQ range is restricted to ±6dB in each frequency band. This is continouusly variable in the statically programmable unit, and adjustable over the same range in 1.5dB increments when the Processor is under optional computer control.

FM Peak Limiter (250-00)

A split-band approach to final peak control is utilized for FM and TV-aural broadcasting. This limiter option has application in STL systems and in some production and recording situations as well. As delivered, the frequency-selective nature of the limiter ceiling characteristic accommodates the normal 75-microsecond pre-emphasis curve. This can, nontheless, be restrapped for a 25- or 50-microsecond or a flat characteristic.

The split-band technique is block-diagrammed in Figure 4. The Broadband audio is divided into two components, one representing the portion of the spectrum which is pre-emphasized in transmission, the other component consisting of the signal which is not pre-emphasized. Each band is independently limited so that program energy never exceeds the ceiling limit imposed by the transmission pre-emphasis curve.

Energy at the lower frequencies is controlled only by the level of the lower band. The pre-emphasized frequencies, however, are controlled both by energy within that band and by that of the lower band. Thus high frequency peaks (such as a cymbal crash) will be reduced without creating an audible "hole" in the broadband program level, yet voice (and lower) frequency peaks will reduce overall broadband gain and retain the program

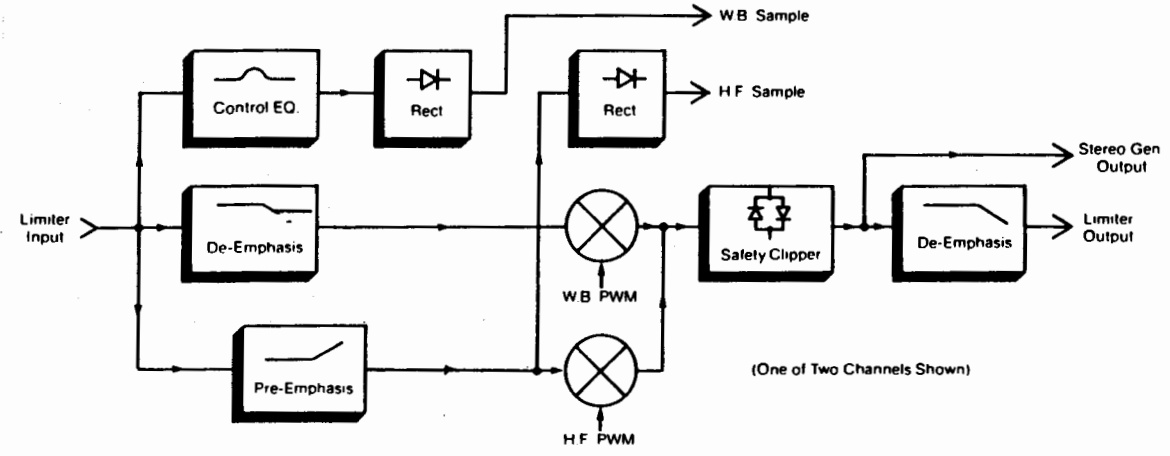


Figure 4 - Block Diagram, FM Peak Limiter

tonal balance. If this were not the practice, the program would sound artificially "bright."

Peak Limiter gain control is accomplished with a feedforward technique similar to that utilized in the multiband compressor circuit. The transfer function, graphed in Figure 5, is semi-abrupt, however, with an infinite final ratio.

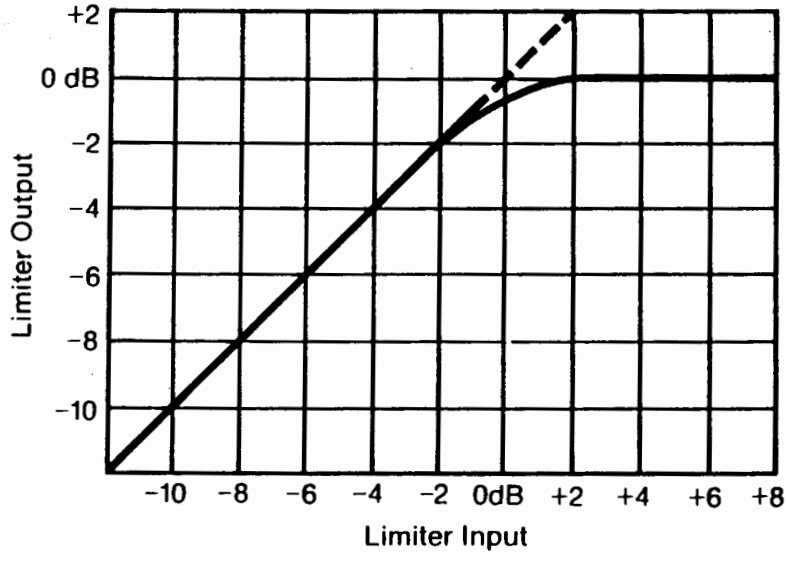


Figure 5 - Peak Limiter Transfer Function

Limiter attack is virtually instantaneous in both frequency bands. Release timing, on the other hand, is optimized for fast operation consistent with low signal distortion. This means that the high frequency limiter, which never deals with frequencies below about 1kHz, can have a very quick release time. The broadband peak limiter release timing, however, is a complex, program-derived function. The average value of the limited peaks establishes a floating "platform" characterized by a slow recovery. Occasional fast peaks, however, will result in a rapid release from the instantaneous reduction figure to the platform value. This dual-slope limiter release characteristic lessens the tendency toward "pumping" and other objectionable side-effects of heavy final limiting.

The left and right limiters track one another, both for broadband and for independent high frequency peak reduction. Limiting is based on the higher of the L or R signals, and is user-programmable at 2, 4, 6, 8 or 10dB, nominal.

A final "safety" clipper, which also conforms to the pre-emphasis curve, is included in the peak control circuitry. This clipper does not normally act on program material, but guards against certain fast overshoots which can occur as the limited broadband and high frequency program components are recombined.

The Processor line output has a flat, not a pre-emphasized characteristic. The normal pre-emphasis imparted by the transmitter or stereo generator satisfies the transmission system requirement.

AM Peak Limiter (250-01)

The Motorola C-QUAM AM-stereo system, generally recognized as the standard system, worldwide, is mono-compatible; that is, the L+R program signal amplitude-modulates the broadcast transmitter for monaural reception with existing receivers. The L-R program information, on the other hand, is transmitted as a form of carrier phase modulation.

Unlike FM-stereo with a subcarrier contributing to, and imposing restrictions on, total (mono) modulation, AM-stereo permits full L+R (amplitude) modulation in addition to a L-R (phase) modulation component. To gain maximum modulation advantage, especially for the monaural signal, peak processing must be done in a matrixed mode. Simple left-only and right-only processing, even with L/R correlation, could restrict the AM (mono) signal to something less than full, 100%-plus modulation.

The Inovonics 250 AM Peak Limiter (Figure 6) is fully matrixed. The left and right channel signals are combined into L+R and L-R components and separately limited for full modulation ad-

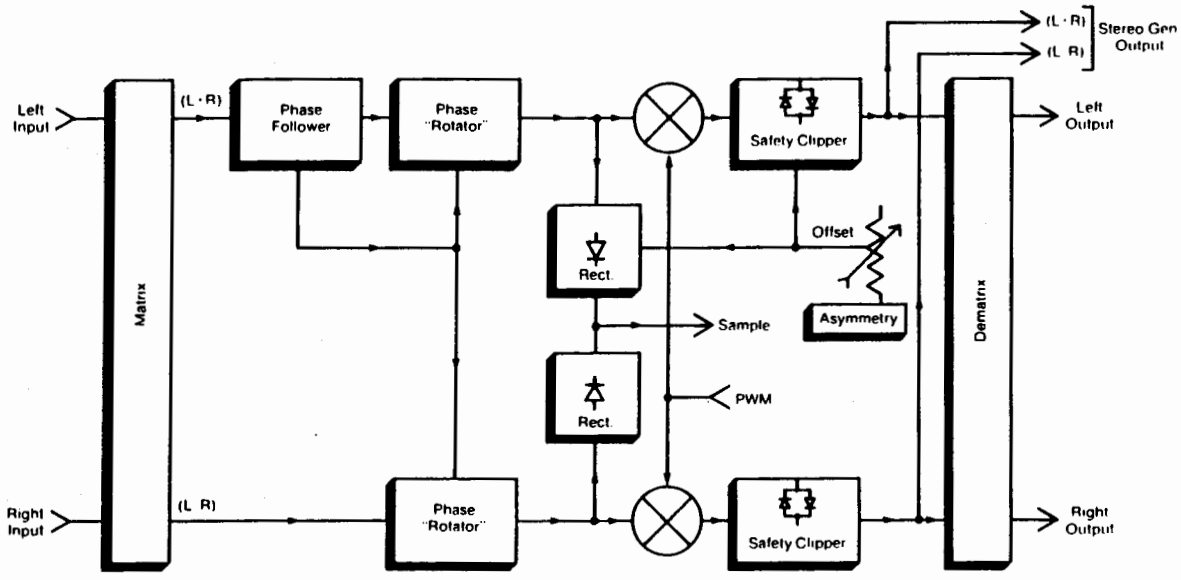


Figure 6 - Block Diagram, AM Peak Limiter

vantage. In addition, the L+R (mono) signal is capable of phase-following, asymmetrical carrier modulation with positive peak excursions to +125%. A phase "rotator" circuit puts the L+R and L-R signals through a simultaneous 180-degree "roll" as required to maintain maximum positive peak energy in the L+R channel. Absolute tracking of the two phase rotation circuits assures that the stereo relationship is preserved.

The AM limiter has the same transfer characteristic (Figure 4) and floating "platform" release function of the broadband channel of the FM limiter. AM limiting is strictly broadband, however, no separate high frequency limiter is used. Limiting is based on the higher of the L+R or L-R program components and is user-programmable at 2, 4, 6, 8 or 10dB, nominal.

Once the stereo program is limited in the matrixed mode, the L+R and L-R signals are dematrixed to yield discrete left and right program line outputs. Nevertheless, when rematrixed by the AM stereo generator, the matrix-mode processing restrictions and advantages still apply.

Static Processor Programming

The standard, static programming card (A/N 164200) implements the various processing parameter presets for A.G.C., compression, equalization and final limiting. Five programmable formats are

identified "A" through "E."

Format "A" is factory-programmed for a "typical" broadcast situation and can be thought of as a "reference standard" when setting up the other formats.

FORMAT "A" PROGRAMMING	
A.G.C.	ON
Compression	6dB
Equalization	FLAT
Limiting	4dB

Formats "B" through "E" may be preset for the parameter programming options specified in the Functional Descriptions of the various Processor elements.

A "PROOF" mode defeats all gain control functions and equalization, yet leaves the audio signal path intact at a unity-gain value.

The five formats and the PROOF mode are selected by a series of contact closures to ground. Three control lines address the six functions with BCD logic encoding. Two simple switching circuits for manual format selection are diagrammed in Section III, Page 18. Alternately, relay contact closures or open-collector NPN transistor switches can be used for remote control.

The static programming circuit card has an on-board rotary selector switch to facilitate Processor setup. When the card is pulled out for adjustment (this is made possible by a spring-retracted interconnect cable) the remote address commands are inhibited and the on-board selector switch has format selection priority. The reverse is true when the card is re-inserted in its normal position.

Setup information for the static programming card is contained in Section IV, Page 24.

Computer Interface Programming Option (A/N 169200)

The static programming card supplied with the Inovonics 250 may be replaced at any time with an optional interface assembly to put the Processor under external computer control. Programmable parameters may then be continuously updated to accommodate even more station programming variables. Depending upon the complexity of user-written software, the Processor may be integrated with station automation, program spectral dynamics, time of day, etc.

The interface assembly is controlled by an RS-232C serial data bus, probably the most universal computer interface standard.

It is certainly not within the scope of this manual to address the subject of computer programming; that will depend on the computer used, the desired process control functions, etc. Formatting of the digital control data and some of the operational factors which will influence programming are covered in Section V.

Specifications

Those performance specifications of the Inovonics 250 which are not specifically expressed in the text of the discussions or in the attendant drawings are tabulated here:

Frequency Response (below Compressor and Limiter thresholds: ±0.5dB, 10Hz - 15kHz

Noise*: better than 70dB below 100% modulation, 10Hz - 20kHz

Crosstalk*: better than 60dB below 100% modulation, 10Hz - 20kHz

Distortion*: under 0.5%, 20Hz - 15kHz; under 0.2%, 50Hz - 10kHz

Inputs: LEFT and RIGHT; balanced-bridging, -20 to +10dBmV.

Outputs: LEFT, RIGHT and MONO; balanced, 0 to +15dBm (into 600-Ohm load)

Power: 105 - 130VAC (230V available); 20W, 50 / 60Hz.

Size: 5-1/4" x 19" x 8" overall

Shipping Weight: 11 lbs.

* Data taken with Processor gain adjusted for 10dB Compression and 10dB Limiting of typical program material.

III INSTALLATION

Unpacking and Inspection

Upon receipt of the equipment, inspect at once for shipping damage. Should any such damage be observed, notify the carrier; if not, proceed as outlined below. It is suggested that the original shipping carton and materials be retained should future reshipment become necessary. In the event of return for Warranty repair, shipping damage sustained as a result of improper packing for return may invalidate the Warranty.

> IT IS IMPORTANT that the Warranty Registration Card found at the front of this manual be returned. Not only does this assure coverage of the equipment under terms of the Warranty and provide some means of trace in the event of equipment theft, but the user will automatically RECEIVE SPECIFIC SERVICING OR MODIFICATION INFORMATION should it be issued by Inovonics.

Mounting

The Inovonics 250 is packaged to mount in a standard 19-inch equipment rack and requires 5-1/4 inches of rack space. The 250 generates negligible heat, and itself is unaffected by wide variations in the ambient operating temperature.

AC Power

Unless it has been special-ordered for export shipment, the 250 is designed to operate from 115V, 50/60Hz AC mains power. If supplied for 230V operation, the unit will be so identified on the rear panel near the AC connector. Note that the value of fuse has been specified on the rear panel for each line voltage.

The power cord is fitted with a North American-standard male connector, but the individual cord conductors are color-coded in accordance with CEE standards. (BROWN: "hot", BLUE: neutral, GREEN/YELLOW: ground.)

RFI

The Inovonics 250 is specifically designed to operate in close proximity to broadcast transmitters; nevertheless, care should be exercised in locating the unit away from abnormally high RF fields.

In some installations situations an RF ground loop may be formed between the input or output cable shield grounds and the AC power cord ground. Use of a "ground-lifting" AC adapter should remedy the problem, but the chassis of the unit should somehow be returned to earth ground for safety.

Line Inputs and A.G.C. Board Strapping

The Inovonics 250 has separate left and right electronically-balanced (transformerless) bridging inputs. These are brought out to the rear panel barrier strip and include a chassis ground connection for cable shields.

Should the equipment which feeds the Processor require output loading, a 600-ohm terminating resistor may be placed across the input terminals.

The "+" and "-" input terminal designations remain in phase with line output terminals similarly identified. If the 250 is fed single-ended, connect the signal to the "+" terminal and strap "-" to ground.

The unit accepts zero-reference input program levels between -20 and +10dBm. This input range is divided into two parts. As shipped, the 250 will take input levels between -5 and +10dBm. To change the input range for program levels between -20 and -5dBm, the four "A" straps on the A.G.C. board must be installed. These strapping points are near the top-rear of the A.G.C. board.

NOTE: Model 250-02 Processors (monaural AM) use only the left channel input terminals for the mono program feed.

FM Peak Limiter Jumpering Options (250-00)

The left and right FM peak limiter cards (A/N 194500) are identical. Each has a series of four jumper terminals to select the frequency-selective nature of the peak control function.

When the two terminals marked "75" are jumpered, high frequency limiting will conform to the 75-microsecond characteristic. Similarly, jumpering the two terminals marked "50" will yield a 50-microsecond limiting characteristic.

Although the limiter output ceiling conforms to the selected characteristic, the output program signal is not pre-emphasized. Pre-emphasis is normally imparted by the stereo generator or FM exciter.

AM Peak Limiter Jumpering Options (250-01 and 250-02)

The AM-stereo peak limiter is comprised of two P.C. cards, A/N 168100 for the L+R matrixed signal, and A/N 168101 for the L-R component. The two cards differ only in the way they are jumpered, the last two digits of the assembly number corresponding to jumper positions. It is important that the L+R board (00 jumpers installed) is plugged into the left-hand limiter slot, the L-R board (01 jumpers) into the right-hand slot. (This is shown on the inside of the 250 front cover.)

The 02 jumper positions are for monaural AM operation in Model 250-02 Processors specifically delivered for mono-AM use. In this case the A/N 168102 board is plugged into the left-hand slot and the monaural output taken from the LEFT LINE OUTPUT terminals.

Stereo Line Outputs

The left and right line outputs appear at the rear panel barrier strip along with ground terminals for cable shields. Outputs are electronically balanced (transformerless) but not load-sensing. They will drive the balanced inputs of stereo generators and transmitters or normal program lines.

> If a single-ended output is required, only the "+" and "GND" terminals should be used; the "-" side should not be grounded.

The characteristic output impedance of the 250 is 600-ohms. When terminated in a similar value of resistance, the output level will be 6dB below the unloaded value. The outputs are variable between 0 and +15dBm into a terminated, balanced load.

Line outputs are designated "+" and "-" for program phase considerations, and are in phase with the similarly-designated line input terminals. In AM-stereo use, it is important that positive-going waveforms on the "+" terminals result in positive amplitude modulation of the transmitter.

Mono Line Output

A L+R monaural line output is available for monitor or for interim AM or TV use. This output has the same characteristics as the left and right outputs, except that it must be used in the balanced mode only.

Remote Control of Static Programming

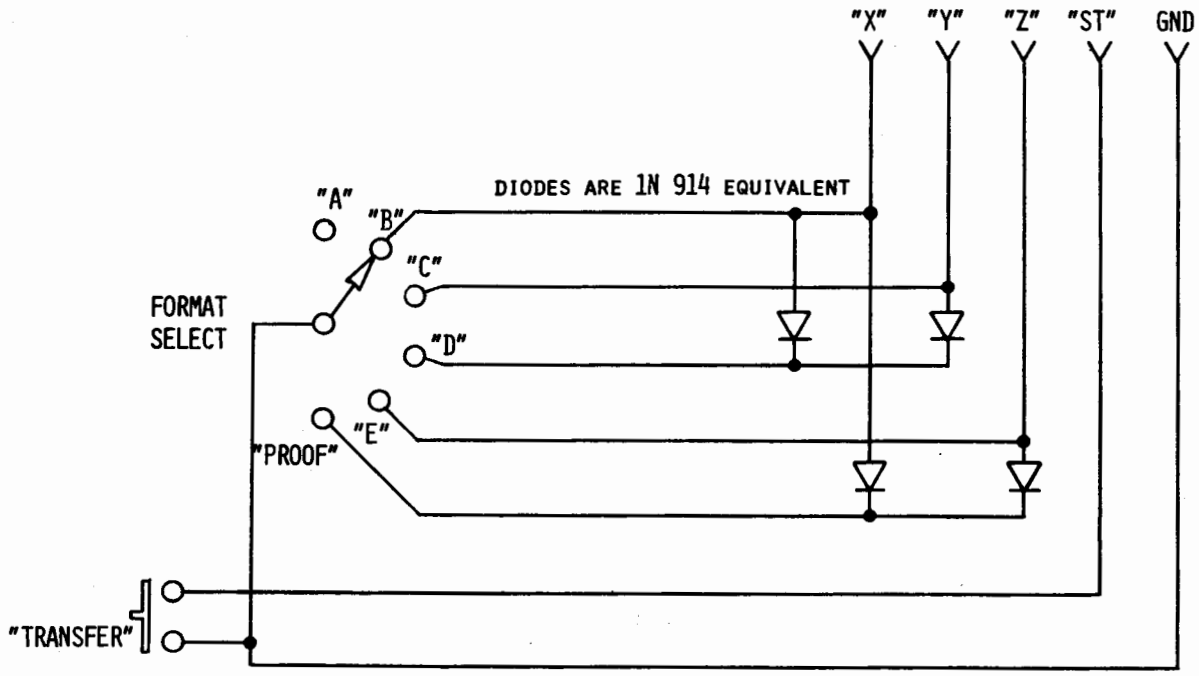
The static programming assembly (A/N 164200) is addressed by a coded command to call up the different processing presets. The rear panel barrier terminals "X," "Y, "Z" and "ST" constitute a strobed, BCD control input port which is coded as shown below.

MODE	"X"	"Y"	"Z"
A	0	0	0
B	1	0	0
C	0	1	0
D	1	1	0
E	0	0	1
PROOF	1	0	1

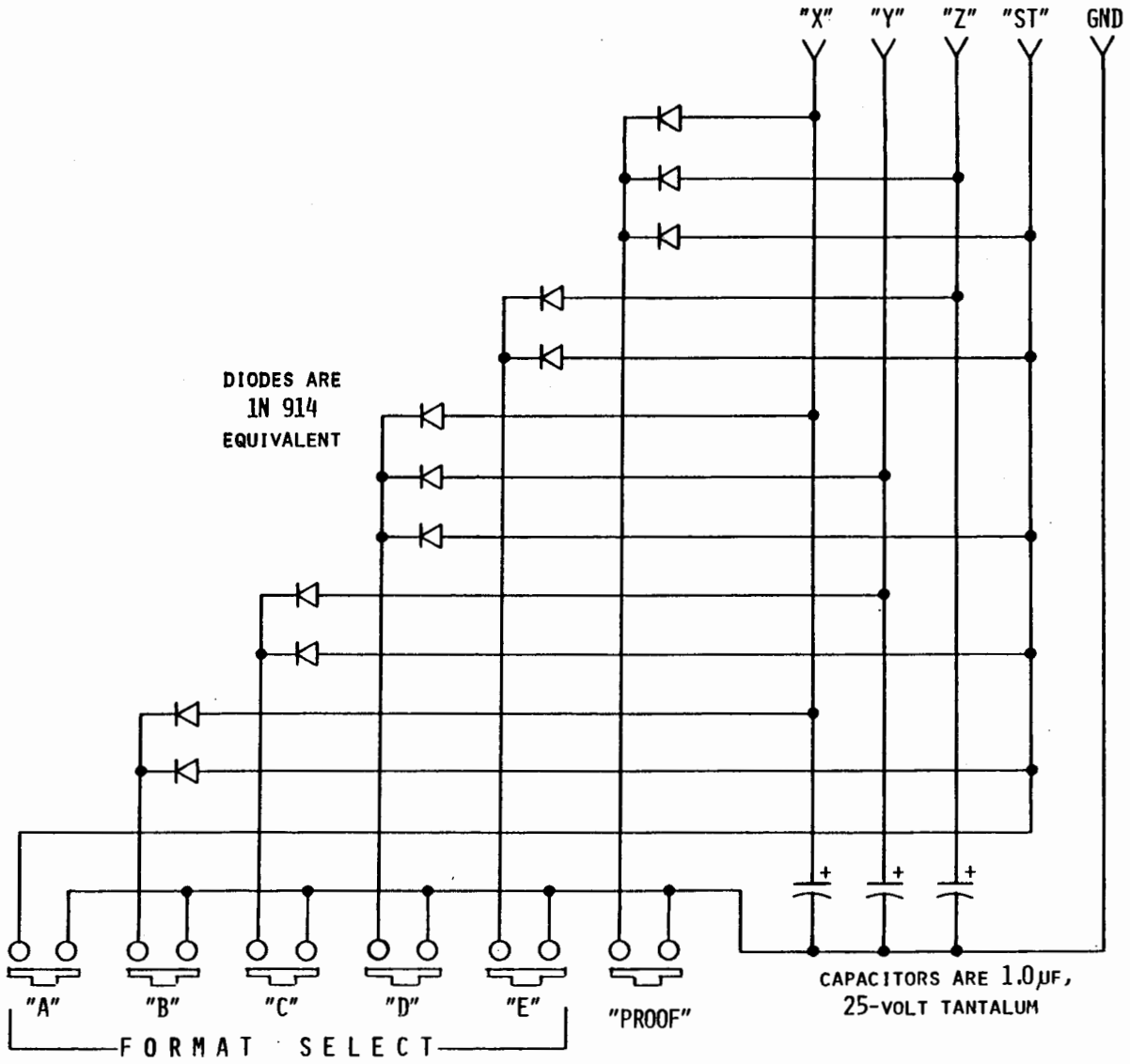
0 = open; 1 = ground

When the three address lines are brought to ground and the "ST" (strobe) line is momentarily grounded, the address command will be entered. This utilizes a built-in memory in the programming assembly. Alternately, the "ST" line can be permanently strapped to ground and the three address lines selectively held at ground to maintain the address command. This is a somewhat more reliable control technique and assures that the command will not be lost during a power outage.

Two simple control switching schemes are shown here; one for a rotary selector, the other utilizing momentary pushbuttons. Nearly any design can be used with either switch or relay contacts, saturated NPN transistors or open-collector TTL devices.



(TRANSFER FUNCTION IS OPTIONAL; PROVIDE A PERMANENT SHORT IF THIS FUNCTION IS NOT DESIRED)


"X"
"Y"
"Z"
"ST"
GND
DIODES ARE
1N 914
EQUIVALENT
"A"
"B"
"C"
"D"
"E"
"PROOF"
FORMAT SELECT
CAPACITORS ARE 1.0μF,
25-VOLT TANTALUM

IV SETUP AND OPERATION

With the exception of the Processor programming controls, which are entirely contained within the static programming assembly, the Inovonics 250 has only input and output level controls for the left and right channels. Setup of the Processor is simple and straightforward. The only test equipment required is a 500Hz, sinewave signal source which can be routed through the audio console. Most setup is performed with the Inovonics 250 "on-air" in the normal broadcast chain.

Input Gain Set

STEP 1 Apply a 500Hz sinewave test signal to both the left and right inputs of the Processor from the audio console or from whatever other equipment directly feeds the unit.

STEP 2 Adjust the level of the test tone for a value exactly 1.5dB above the normal program "zero" level.

A. This would be +9.5dBm if 0 VU = +8dBm; +5.5dBm if 0 VU = +4dBm.

B. A +1.5 VU indication on the console meter is sufficiently accurate.

STEP 3 Select the "A" processing format with the local selector switch on the static programming card (see Page 13).

STEP 4 Turn the RIGHT INPUT "OFF" with the appropriate switch on the A.G.C. card. The LEFT INPUT should be "NORMAL."

STEP 5 Adjust the LEFT INPUT GAIN control to a point which causes both the 0dB and -3dB A.G.C. GAIN indicator LED's to light evenly.

A. This step must be performed slowly because of the very slow A.G.C. correction rate.

B. If this adjustment is not within the range of the control, consult Page 16 for A.G.C. re-strapping instructions.

STEP 6 Switch the LEFT INPUT "OFF" and the RIGHT INPUT to "NORMAL." Repeat STEP 5 for the RIGHT INPUT GAIN control.

STEP 7 Return both INPUT switches of "NORMAL" and reduce the

500Hz test signal to normal program "zero" level. The A.G.C. GAIN indicator should register 0dB.

Output Level Set, FM Version (250-00)

This procedure is best performed "on-air" using the station Modulation Monitor and a 500Hz sinewave test signal from the audio console. Alternately, the 500Hz tone generator in the Inovonics 250 may be used.

STEP 1 Select the "B" processing format with the local selector switch on the static programming card (see Page 13).

STEP 2 Preset the "B" format as follows:

A. A.G.C.: ON

B. ALL "DIP" SWITCHES: ON

C. ALL EQUALIZATION CONTROLS: FULL CW (+6dB)

STEP 3 Apply the 500Hz test signal to the LEFT input only (RIGHT INPUT "OFF").

A. LEFT INPUT "NORMAL" if tone comes from the audio console.

B. LEFT INPUT "TEST OSC" and TEST OSCILLATOR FREQUENCY to "500Hz" if the internal source is used.

STEP 4 The Processor should show 8-10dB of broadband limiting. The LEFT CHANNEL LINE OUTPUT control can now be adjusted for 100% modulation of the transmitter as monitored by the station Modulation Monitor.

STEP 5 Switch the LEFT INPUT "OFF" and apply the tone to the right channel of the Processor.

STEP 6 Adjust the RIGHT CHANNEL LINE OUTPUT level control for 100% modulation.

STEP 7 Switch both the LEFT INPUT and RIGHT INPUT to "NORMAL" (or to "TEST OSC") so that both channels are driven by the test tone. The modulation level should remain at 100%.

A. If some form of composite clipping is employed to control overshoot of the low-pass filter in the stereo generator, the clipping threshold can be adjusted at this time to "just barely touch" the peaks of the composite signal. Such adjustment will insure that only the overshoot products of the filter are clipped.

B. If there is no provision to control LPF overshoot, both the LEFT and RIGHT CHANNEL LINE OUTPUT controls

will have to be backed-down to avoid overmodulation of the carrier by overshoot products. The amount of level reduction (which will, of course, result in a loss of average audio modulation) will have to be determined experimentally, as it will depend on the stereo generator LPF characteristics.

Output Level Set, AM Version (250-01)

This procedure is best performed "on-air" using the station Modulation Monitor and a 500Hz sinewave test signal from the audio console. Alternately, the 500Hz tone generator in the Inovonics 250 may be used.

STEP 1 Select the "B" processing format with the local selector switch on the static programming card (see Page 13).

STEP 2 Preset the "B" format as follows:

A. A.G.C.: ON

B. ALL "DIP" SWITCHES: ON

C. ALL EQUALIZATION CONTROLS: FULL CW (+6dB)

STEP 3 Turn the POS. PEAK AMPLITUDE control on the L+R peak limiter card (left-hand limiter board) fully CCW. (The corresponding pot on the other limiter card is defeated and has no effect on Processor operation.)

STEP 4 Apply the 500Hz test signal to the LEFT input only (RIGHT INPUT "OFF")

A. LEFT INPUT "NORMAL" if tone comes from the audio console.

B. LEFT INPUT "TEST OSC" and TEST OSCILLATOR FREQUENCY to "500Hz" if the internal source is used.

STEP 5 The Processor should show 8-10dB of broadband limiting. The LEFT CHANNEL LINE OUTPUT control can now be adjusted for 100% amplitude modulation of the transmitter as monitored by the Modulation Monitor.

STEP 6 Switch the LEFT INPUT "OFF" and apply the tone to the right channel of the Processor.

STEP 7 Adjust the RIGHT CHANNEL LINE OUTPUT level control for 100% modulation.

STEP 8 Switch both the LEFT INPUT and RIGHT INPUT to "NORMAL" (or to "TEST OSC") so that both channels are driven by the test tone. The indicated limiting will increase to approximately 20dB, but there should be no change in indicated transmitter amplitude modulation. If modulation does increase slightly, back down both the LEFT and

RIGHT CHANNEL LINE OUTPUT controls symmetrically to return to 100% modulation.

STEP 9 Set the Processor to the "A" format and apply a normal stereo program signal from the audio console. The POS. PEAK AMPLITUDE control may now be adjusted for positive peaks up to +125%.

STEP 10 Whatever provision is made for adjusting the carrier phase (L-R) modulation may also be done at this time.

HINT: Reversing the phase of one audio channel ahead of the Processor input will increase the L-R (difference) component and facilitate this adjustment.

Following the Processor output adjustment, be sure to re-program the "B" format.

Static Processor Programming

The static programming card may be withdrawn with its retractable, captive cable assembly during Processor operation. The remotely-selected processing format will, however, temporarily revert to whatever the on-board format selector switch has been set to.

Controls for the four programmable formats are identified on the metal faceplace which covers part of the static programming card.

The five equalizaion controls, identified 1 through 5, correspond to the five bands of compression called out on the front panel. The ±6dB markings around the pots are approximate; adjustment is usually made "by ear."

The ±6dB range restriction does, of course, translate into a 12dB overall spread. Should, for instance, a 10dB boost at midband frequencies be required (eg: for an ENG audio feed), the top and bottom can be cut by 4dB to increase a 6dB mid boost to 10dB.

A.G.C. is turned on or off for the "B" through "E" formats with the #1 switch position. As shown on the faceplate, the ON position for each DIP switch is "down," toward the edge of the board.

IMPORTANT: The compression and limiting switches must be progressively turned on for the desired value. Compression is increased in 3dB steps, starting with switch position #2 for an additional 3dB over the minimum 3dB value, then position #3 for another 3dB, etc. Peak limiting is selected the same way, always with the first switch in the series closed before the next. Random switch selection will not result in the degree of processing indicated.

Parameter changes are normally made on a subjective listening basis and should be done slowly, with forethought and care. Always compare results with the "A" format to check against a "typical" setup, or against PROOF for a totally unprocessed signal.

V COMPUTER CONTROL OF THE INOVONICS 250

The optional dynamic programming assembly (A/N 169200) implements the same Processor control functions as the standard static programming card, except that it accepts computer-generated commands via the RS-232C serial data bus.

Actual computer programming cannot be covered here in depth; however, the subjects of address formatting and some aspects of Processor control must be understood before a working computer program can be written.

RS-232C Bus Connection

When the dynamic programming card is installed in the Inovonics 250, the rear-panel barrier strip terminal marked "X" becomes the serial data receive line; "Y" is digital ground.

Baud Rate Selection

The dynamic programming assembly can be strapped to receive serial data at 150, 300, 600, 1200, 2400, 4800 or 9600 baud. The rate must, of course, correspond to that of the controlling computer. It is selected by installing a shorting jumper wire strap across the appropriately marked terminals of J4, near the front edge of the card. As shipped, the assembly is strapped for 1200 baud.

Data Error Indication

The assembly is a receive-only interface. Since it can receive and process the serial input data immediately, even at the highest baud rate, no information need be returned to the controlling computer.

With principal respect to the RS-232C bus format, however, the Inovonics 250 provides an error indication should the received data fail to conform to the proper format in these respects:

FRAMING ERROR

PARITY ERROR

INPUT REGISTER OVERRUN

The rear-panel barrier strip terminal marked "Z" normally sits "high" at +5 volts. Should data errors be detected, the "Z" terminal will be pulled to the same potential as the digital ground terminal, "ST."

RS-232C Data Bus Format

Although it represents a data communications standard for computers, modems, printers and other digital equipment, the RS-232C serial data bus has certain format variables which must be compatibly structured for the Inovonics 250. These format variables are:

8 BITS-PER-CHARACTER

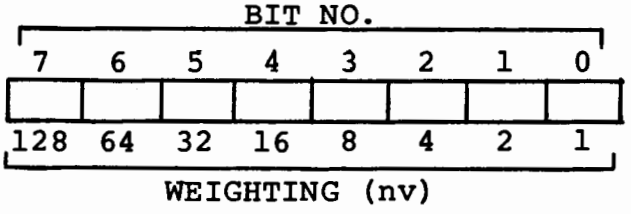
2 STOP BITS

ODD PARITY

In some cases these variables are set by switches or jumpers within the computer or its interface peripheral. Alternately they could be under some form of software control. Consult the computer manual for interface and output port specifications.

Control Function Formatting

The Inovonics 250 receives input digital data in the form of an 8-bit "byte." This byte, diagrammed below, consists of bits 0 through 7, least-to-most significant, respectively.



A numerical, binary-weighting value is shown below each bit. Through binary addition, the eight bits can represent any number between 0 and 255. For example:

0 0 1 0 0 1 1 0 = 38

With computers using the BASIC language, Processor control commands will be derived from computer "PRINT" functions conforming to the ASCII code. The binary-weighted numerical value (nv) of each ASCII character constitutes the CHR$ (Character String) code. This value is the same as the 8-bit Processor control byte value. For example, a possible computer instruction: PRINT CHR$(38); would give a direct Processor control command of: 0 0 1 0 0 1 1 0.

NOTE: The semicolon (;) following the print command in the example is typical of an extra character usually required to prevent an automatic carriage return which would otherwise void the data.

Consult the computer manual to verify proper CHR$ formatting

For the purpose of programming the Inovonics 250, the 8-bit byte can be thought of as two, 4-bit blocks. The first block, starting with the least significant bit, assigns dB values to compression, equalization and limiting. The second block, ending with the most significant bit, is the function address code for the first block.

The table on the following page diagrams the various Processor control functions in terms of the 8-bit digital command. To arrive at a CHR$ code, add the numerical values (nv) of the first and second data blocks.

An example:

Desired Processing Variables:

```
A.G.C.: ON
Compression: 6dB
Band 1 EQ: -3dB
  "   2 EQ:  0dB
  "   3 EQ: +1.5dB
  "   4 EQ: +4.5dB
  "   5 EQ: +3dB
Limiting: 8dB
```

Computer Command:

```
PRINT CHR$ (83);(1);(19);(36);
(54);(69);(103);
```

The dynamic programming assembly utilizes data latches to maintain a programming command until that function is again addressed and updated. This means that the Processor must initially be "loaded" with a full set of parameter variables once power is applied.

PROCESSOR CONTROL FUNCTION FORMATTING TABLE

ADDRESS	(nv)	BLOCK 1		BLOCK 2	(nv)	dB ASSIGN
A.G.C. and COMPRESSION	(80)	0 1 0 1	+	0 0 0 0	(0)	A.G.C. OFF, 3dB COMP
				0 0 1 0	(2)	" " 6dB "
				0 1 1 0	(6)	" " 9dB "
				1 1 1 0	(14)	" " 12dB "
				0 0 0 1	(1)	A.G.C. ON, 3dB "
				0 0 1 1	(3)	" " 6dB "
				0 1 1 1	(7)	" " 9dB "
				1 1 1 1	(15)	" " 12dB "
EQ, BAND 1	(0)	0 0 0 0	+	1 0 0 0	(8)	-6dB
EQ, BAND 2	(16)	0 0 0 1		0 0 0 0	(0)	-4.5dB
EQ, BAND 3	(32)	0 0 1 0		0 0 0 1	(1)	-3dB
EQ, BAND 4	(48)	0 0 1 1		0 0 1 0	(2)	-1.5dB
EQ, BAND 5	(64)	0 1 0 0		0 0 1 1	(3)	0dB
				0 1 0 0	(4)	+1.5dB
				0 1 0 1	(5)	+3dB
				0 1 1 0	(6)	+4.5dB
				0 1 1 1	(7)	+6dB
PEAK LIMITING	(96)	0 1 1 0	+	0 0 0 0	(0)	2dB LIMIT
				0 0 0 1	(1)	4dB LIMIT
				0 0 1 1	(3)	6dB "
				0 1 1 1	(7)	8dB "
				1 1 1 1	(15)	10dB "

Programming Hints

The Inovonics 250 is able to respond instantly to programming commands. If programmed changes are made in incremental steps, they will be inaudible under nearly all listening conditions.

> For instance: to go from 3dB to 12dB of Compression, cycle through the intermediate steps over a period of 2 - 3 seconds.

Since a power failure will result in loss of control data held in the internal latches, it is suggested that a "standard" Processor control program be maintained in non-volatile computer memory with automatic provision to load the program into the Processor upon restoration of power.

Similarly, if the Inovonics 250 is located at a remote transmitter site and controlled via modem, an occasional data "refresh" would guard against data error or loss due to line facilities failure.

PROOF Mode

Under computer control, the Inovonics 250 is placed in PROOF through a series of eight bytes. These are:

FUNCTION	COMMAND	(nv)
BAND 1 EQ: FLAT	0 0 0 0 0 0 1 1	(3)
" 2 " FLAT	0 0 0 1 0 0 1 1	(19)
" 3 " FLAT	0 0 1 0 0 0 1 1	(35)
" 4 " FLAT	0 0 1 1 0 0 1 1	(51)
" 5 " FLAT	0 1 0 0 0 0 1 1	(67)
A.G.C.: OFF; MIN COMP GAIN	0 1 0 1 0 0 0 0	(80)
MINIMUM LIMITER GAIN	0 1 1 0 0 0 0 0	(96)
DISABLE *	0 1 1 1 0 0 0 1	(113)

* The last byte shown (113) is the one which DISABLES the compression and limiting functions. If the Processor has once been put in PROOF, the DISABLE command MUST BE TURNED OFF when normal operation is resumed.

This is done with the command:

0 1 1 1 0 0 0 0 (112)

VI CIRCUIT DESCRIPTIONS

This section describes the circuitry used in the Inovonics 250. The discussions refer to the schematic diagrams, all of which are contained in the Appendix.

Since its use is unique to the Model 250 Processor, the first part of this section covers the general subject of Pulse Width Modulation (PWM), and, specifically, its implementation in the 250. Signal path circuitry discussions then follow.

Pulse Width Modulation

PWM is utilized exclusively for audio gain control throughout the Inovonics 250. It is perhaps the most simple and colorless means of varying the amplitude of an analog signal with a DC control voltage.

Consider an audio signal which can be turned on and off with a toggle switch. When the switch is ON, attenuation is zero; when OFF, attenuation is infinite. If this switch can be turned on and off at a rate at least twice that of the highest audio frequency, linear signal attenuation becomes directly proportional to the OFF time.

ON	OFF	dB ATTEN
100%	0%	0dB
50%	50%	6dB
25%	75%	12dB
10%	90%	20dB
1%	99%	40dB
0%	100%	(infinite)

This technique gets a bit touchy at small duty cycles (40dB or more attenuation), relegating it to uses which do not require great amounts of attenuation. PWM thus lends itself well to audio processors because it is easily implemented and very predictable over the 0 - 30dB attenuation range required.

The switching frequency used in the Inovonics 250 is 100kHz; better than 6 times the highest audio frequency passed. Relatively simple low-pass filters prevent "aliasing" and remove

the switching frequency component from the output signal.

The actual pulse width modulation of the audio signal is performed by CMOS Quad Bilateral Switches. These are operated between the ±6-volt supply rails to pass ground-referenced audio signals without distortion.

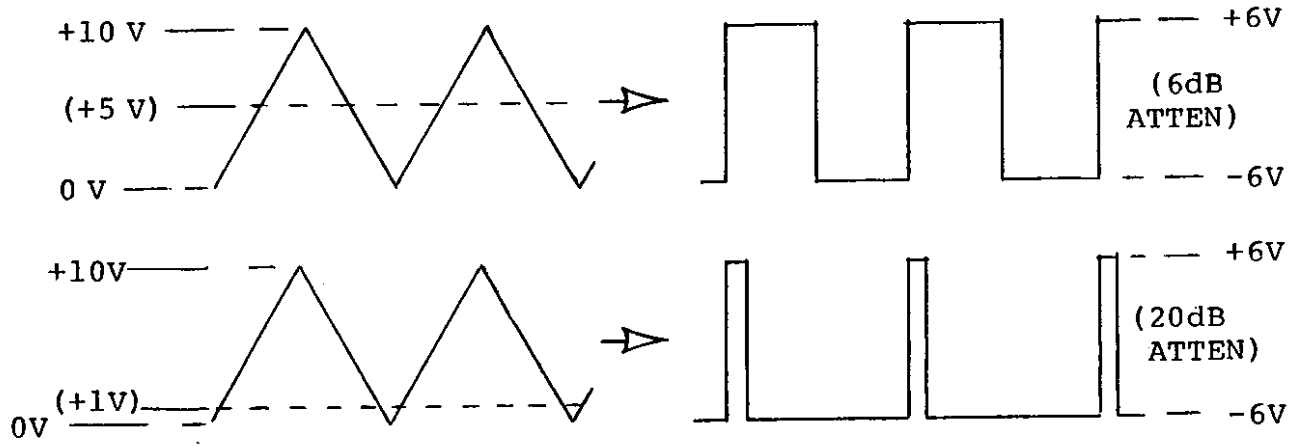
PWM Assembly (A/N 164400; Schematic 170000, Page 56)

This circuit card contains a 10-volt reference source, IC11; a 100kHz precision triangle generator, IC9 and 10; and eight, independent PWM encoders, IC1 through 8.

The 10-volt reference is used by several circuit assemblies in the Processor. +10 volts corresponds to a DC level-controlling voltage representing zero attenuation. With reference to the 10-volt source, a 5-volt control voltage would result in 6dB attenuation, 1 volt yielding 20dB. The 10-volt value serves as a reference from which control voltages are derived, and need not be absolute.

IC9 and C6 form an integrator which feeds comparator, IC10. Hysteresis provided by FET, Q9, causes IC10 to toggle back and forth, driving the integrator in an opposite direction each time. The overall action is that of a free-running, high-linearity triangle generator with a positive peak value equal to the 10-volt reference, and a negative peak value of 0 volts.

The triangle wave is applied to one input of each PWM-encoder comparator IC, IC1 through 8. The other comparator input receives a DC control voltage representing the amount of required signal attenuation in each case. The comparator output is a 100kHz squarewave, the duty cycle (ON vs. OFF) corresponding to the intercept point of the control voltage on the triangle.



Each comparator also provides level shifting and incorporates a current-gain bootstrap stage to maintain fast rise and fall times.

Log Function Converter (A/N 164600; Schematic 170100, Page 55)

With exception of the slow A.G.C. function, the gain-control circuits of the Inovonics 250 are an open-loop, feedforward design. The gentle transfer characteristic of the compressor is plotted in Figure 3, Page 8; the more abrupt peak limiting curve shown in Figure 5, Page 10.

Once a desired gain control transfer function (input vs. output) is established, that curve can be used to derive a corresponding relationship between a rectified input signal voltage and a DC control voltage to effect the required dB of gain reduction. This relationship is a semi-log function, and in practice is sufficiently well approximated by segmentation to be within ±0.2dB over a 30dB range. The compression transfer is approximated in 5 segments, the more abrupt and more critical peak limiter function in 7.

Referring to the schematic, the full-wave-rectified input signal from Band 1 is filtered by C1. Time constants of R1, C1 and R7 establish attack and release times for the Band 1 compressor. DC is buffered by Q6 and passed to common-base stage, Q1.

In the OFF condition, the collector of Q1 sits at the +10-volt reference through R12. As current is fed to Q1 through R37, initial voltage gain of this stage is set by R12. When the collector voltage drops to a point where CR1 begins to conduct, R17 also becomes a collector load and the gain of Q1 drops to the "next segment" value. The gain of Q1 continues to decrease as the input current increases, creating the required semi-log relationship. Each collector load diode has a "soft" turn-on characteristic which smoothes the segmentation. A unity-gain, IC buffer isolates each semi-log converter stage.

All five compressor logging circuits are identical, except for the time constants which are set to the optimized values (see discussion starting on Page 6).

The two peak limiter sections have identical semi-log converters, similar to the five compressor circuits. CR35 slaves the high frequency limiter to the wideband channel (see Page 9), and wideband release is the dual-slope function discussed on Page 11. IC4B monitors the difference between the wideband and the high frequency (plus wideband) limiter channels to derive a high frequency (only) display signal.

IC4A is the integrator for the slow A.G.C. Processor function.

As A.G.C. operates in closed-loop fashion, the gain-controlling DC is a direct function of the input DC. The display signal is log-converted for a dB-linear front-panel display.

Peak limiter and A.G.C. DC control outputs are fed directly to their respective PWM encoders. The five compressor control outputs are routed through either the static or the dynamic programming assemblies for post-compression gain (equalization) programming.

Stereo A.G.C. Assembly (A/N 165200; Schematic 170500, Page 51)

The left channel line input is fed to the active-balanced input stage, IC1A. Gain may be set for the input line level range per Page 16. IC1B is a 15kHz, low-pass filter. Gain of this stage is varied by the LEFT INPUT GAIN control, R11. A1(3/4) is one section of a CMOS switch which is driven by the PWM board to provide linear audio gain control. Low-pass filter, IC3A recovers audio from the PWM signal.

Right channel signal circuitry is identical to the left.

Q1 and 2 form a Baxandall full-wave rectifier for the left channel A.G.C. output, Q3 and 4 for the right. The L/R composite is further amplified by Q5 and integrated to a corresponding quasi-peak value by R57 and C21. When A1(10/11) is gated CLOSED, DC is passed for A.G.C. control-rate integration to the log converter assembly.

Overall circuit action adjusts PWM to maintain a quasi-peak-integrated DC value at a figure representing 0dB A.G.C. gain.

IC4B is the frequency-weighted L+R gating signal amplifier. The signal is rectified and fed to IC4A, a hysteretic level detector performing the gate switching function. When A.G.C. is programmed ON, A1(8/9) closes and the function is enabled. A midband signal exceeding the gating threshold closes A1(10/11) and A.G.C. gain is slowly corrected.

IC5B and associated circuitry comprises a Wein Bridge sinewave oscillator which can be switched to either 500Hz or 5kHz. Both the left and the right A.G.C. channels may be manually switched between the input program, the internal oscillator or OFF.

Bandpass Compressor (A/N 194800; Schematic 194600, Page 52)

Input signals from the A.G.C. are fed to programmed-gain stage, IC7A which establishes the drive level to the five compressors. IC7B, the recombining amplifier and output LPF, has a complemen-

tarily programmed GAIN. The net effect is to maintain a constant gain through the compressor assembly, even though the compressors may be programmed to operate on various portions of the transfer curve (Figure 3, Page 8).

Bands 1 and 5 (ICs 4 and 6) are low- and high-pass filters, respectively. Bands 2,3 and 4 (ICs 3,2 and 1) are first-order bandpass filters (see figure 2, Page 8). One section of each op-amp performs the filtering function; the other half is a phase inverter to provide full-wave rectification of the filtered signal. The resultant DC is routed to the log function assembly which establishes the attack, release and transfer characteristics.

Each band filter output is pulse-width-modulated in accordance with the required band gain, both as a function of compression and of programmed equalization.

FM Peak Limiter (A/N 194500; Schematic 194300, Page 53)

Input signals from the compressor are fed to IC9B, a programmed-gain stage which determines the amount of peak limiting.

IC9A imparts 50- or 75-microsecond pre-emphasis characteristics to the program signal in the independent high frequency gain-reduction channel. A shelving de-emphasis around IC8A, the wideband G/R stage, ensures that both signals add to the exact pre-emphasis curve.

The high frequency component is full-wave rectified by IC7 and CR5 and 6 to generate a DC output proportional to the pre-emphasized signal component. Wideband energy is similarly rectifier by IC4 and CR3 and 4, except that a small amount of equalization normalizes control at the -3dB transition frequency.

IC5B and C, controlled by the PWM board, feed the two signal components to LPF combining amplifier IC6B. IC1B further filters the signal which, at this point, still maintains a pre-empahsized characteristic.

CR1 and 2, biased to the proper threshold level by IC3, clip any overshoots which may occur as the WB and HF signal components are combined. The safety clipper is followed by a buffer/low-pass stage, IC1A, the OUTPUT LEVEL control and de-emphasis amplifier IC2A. IC2B inverts the signal phase to provide the active-balanced line output.

AM Peak Limiter (A/N 168100/01; Schematic 170300, Page 54)

> Peak limiting for AM-stereo is performed in a matrixed mode. One board (A/N 168100) limits the L+R signal which amplitude modulates the transmitter. The other board (A/N 168101) limits the L-R signal which phase modulates the carrier. Matrixing, limiting and dematrixing are performed by the board set as a pair, neither board can function independently.

Input signals from both the left and right compressors are fed to IC1B. In the case of the -00 board, these are added to yield a L+R component. In the -01 assembly, they are added out of phase for a L-R signal. IC1A is a programmed-gain stage which determines the amount of peak limiting.

IC8B is a narrowband gain stage driving program peak rectifiers, CR5 and 6. Peaks are held by C15 and 16, then summed at the input of Schmitt trigger, IC8A. The output of IC8A toggles, depending on whether there is a predominance of negative- or positive-going peaks in the midband program waveform. The toggling action is integrated by IC9B and C18 to develop a slow, program phase-rotating ramp between the negative supply and ground. The phase-rotating logic is taken from the L+R (-00) assembly to operate both the L+R and L-R phase rotator circuits. LED I1 and 2 indicate NORMAL or REVERSED status of program phase.

IC2B is a variable-phase-shift amplifier with FET, Q1, the active phase-shifting element. With Q1 biased ON, IC2B is an inverting amplifier which maintains NORMAL program phase. As the gate of Q1 is slowly ramped to pinchoff, the program undergoes gradual phase rotation as IC2B becomes a non-inverting stage. This yields REVERSED program phase. IC2A linearizes Q1 during the rotation period to cancel signal distortion. R20 is trimmed to match the variation in individual FET pinchoff voltages.

IC 3 is a full-wave rectifier for the program signal. IC3A, which rectifies positive program peaks (referred to the line output), may be offset by adjustment of R24 on the -00 (L+R) limiter card. This permits asymmetrical amplitude modulation of the carrier. The offset provision is defeated on the -01 (L-R) assembly.

A2(1/2) is pulse-width-modulated by the PWM board for peak limiter gain reduction. IC4A and B are low-pass filters which remove the PWM switching component.

CR3 and 4, biased to the proper threshold level by IC5, clip

any limiter overshoots. IC5B, which clips positive program overshoots (referred to the line output), is offset on the -00 (L+R) board by the same amount as the program rectifier for asymmetrical carrier amplitude modulation.

IC6A and B dematrix the L+R and L-R signals so that discrete left and right channel outputs appear at the line output terminals. This presupposes that final matrixing is performed in the transmitter.

R50 is the LINE OUTPUT level control. IC7A and B deliver inverted program phases for the active-balanced line output.

Static Programming Assembly (A/N 164200; Schematic 169800, Page 57)

IC7 is a decoder/latch which translates the external format address into BCD control for the analog multiplexers, IC1 through 6. When the card is unplugged from the chassis, address control reverts to the on-board selector switch, S5.

DC control voltages for compressor bands 1 through 5 are routed from the log function board to a series of manually-adjusted equalization controls on the static programming card. The analog multiplexers select the programmed format and feed adjusted DC voltages to the PWM assembly.

Another analog multiplexer, IC6, selects and enables the series of DIP switch assemblies associated with Processor formats "B" through "E." In the "A" and PROOF modes, Processor programming is preset as described on Page 13.

Dynamic Programming Assembly (A/N 169200; Schematics 171100 and 171400, Pages 58 and 59)

The Inovonics 250 computer interface is a two-card, "piggybacked" assembly. Referrring to the schematic on Page 59, incoming RS-232C serial data is buffered by Q3 and fed to IC5, a UART (Universal Asynchronous Receiver/Transmitter). Clock pulses which correspond to the incoming data baud rate are generated on the companion circuit card, buffered by Q2, and also fed to the UART so that data can be properly decoded. IC4 and associated circuitry perform additional timing and reset functions required by the UART when it is used in a receive-only situation such as this. IC3A and Q1 yield an error indication when incorrectly-formatted data is received (see Page 26).

Data output from the UART is a parallel equivalent of the RS-232C serial input byte. IC1 and 2 level-shift the data for CMOS compatibility.

Referring to the schematic on Page 58, IC2 through 6 are CMOS multiplexers which assign programmed equalizer gain to the five compressors. The DC control voltages from the log assembly may be adjusted over a ±6dB range in 1.5dB steps in each of the five bands.

Data latches, IC8 through 12, control the EQ multiplexers; IC13 through 15 provide direct logic outputs. The inputs of all eight latches are presented with the 4-bit "value" byte (see Page 28), and IC7 decodes the 4-bit "address" byte to latch the "value" data as appropriate.

The board also contains IC1, a 12-volt regulator for the CMOS logic, and the baud rate divider and clock, IC16.

VII INTERNAL CALIBRATION ADJUSTMENTS

Through the extensive use of PWM and digital circuit techniques, the Inovonics 250 is unusually free from many of the internal calibration adjustments normally encountered in equipment of this complexity. The few adjustments that are available, however, should not require routine calibration. The following procedures are given in the event that components are ever replaced in areas associated with a claibration adjustment.

Equipment Required

OSCILLOSCOPE: 35MHz bandwidth with low-cap. probe

AC VOLTMETER: -60 to +30dBm full-scale sensitivity

AUDIO GENERATOR: 20Hz - 20kHz; -40 to +10dBm output

EXTENDER CARD (optional): Inovonics A/N 171600

Stereo A.G.C. Assembly (A/N 165200)

The only internal adjustment on this assembly is the STABILITY adjustment for the Wein Bridge test oscillator.

STEP 1 Plug the assembly into the extender card and into the chassis.

STEP 2 Switch the TEST OSCILLATOR FREQUENCY to 500Hz, and both the LEFT and RIGHT INPUTS to TEST OSC.

STEP 3 Monitor the output of the test oscillator with the oscilloscope. The "bottom" of R17 (56K behind the center switch) is a convenient monitoring point.

STEP 4 Adjust R60 for a 16-volt peak-to-peak sinewave.

STEP 5 Switch the TEST OSCILLATOR FREQUENCY to 5kHz. The amplitude should remain unchanged.

STEP 6 Seal R60 with a small dot of Elmer's glue.

NOTE: The small incandescent lamp, I1, is used as a non-linear resistor at very low voltage and does not light.

PWM Assembly (A/N 164400)

The only internal adjustment on this assembly is for the frequency of the precision triangle generator. The actual frequency is not at all critical, and the Processor would operate as well within ±20% of the design center value.

STEP 1 Plug the assembly into the extender card and into the chassis.

STEP 2 Monitor the triangle output with the oscilloscope. The "top" of R17 (100-ohm near the front edge of the board) is a convenient monitor point.

STEP 3 Adjust R20 for 100kHz; one-cycle-per-box at an oscilloscope timebase setting of 10us / div.

STEP 4 Check that the triangle is 10V peak-to-peak and ground-referenced.

STEP 5 Seal R20 with a small dot of Elmer's glue.

FM Peak Limiter (A/N 194500)

This assembly has only the one internal adjustment which sets the threshold level of the peak clipper. This threshold value is set such that the clipper catches limiter overshoots only, and does not affect normal program material.

STEP 1 Plug the left peak limiter assembly into the extender card and into the chassis

STEP 2 Preset the Processor as follows:

FORMAT: "B"
FORMAT "B" A.G.C.: OFF
ALL OTHER FORMAT "B" DIP SWITCHES: ON
ALL FORMAT "B" EQ CONTROLS: FULL CW (+6dB)

STEP 3 Apply a 1kHz sinewave test signal to the LEFT INPUT of the Processor at a level which yields 10dB of wideband peak limiting.

STEP 4 Monitor the output of the clipper buffer stage with the oscilloscope. Pin 1 of IC1 is a convenient monitor point. Sweep the test signal frequency slowly upward until the waveform amplitude peaks. This will be just below the pre-emphasis transition frequency.

STEP 5 Adjust R23 for a slight flattening of the waveform, then back the control off so that no flattening is visible. Seal the trimpot with a dot of glue.

REPEAT THE ABOVE STEPS FOR THE RIGHT CHANNEL. BE SURE TO RESET THE FORMAT "B" PROGRAM WHEN COMPLETED.

AM Peak Limiter (A/N 168100 / 01)

The stereo-AM peak limiter cards always function as a pair, and must be calibrated together. Each card has two internal calibrations, the overshoot clipper threshold and the phase "rotator" matching adjustment.

Clipper Threshold Adjustment

STEP 1 Plug the "left" peak limiter card (A/N 168100) into the extender card and into the chassis.

STEP 2 Preset the Processor as follows:

FORMAT: "B"
FORMAT "B" A.G.C.: OFF
ALL OTHER FORMAT "B" DIP SWITCHES: ON
ALL FORMAT "B" EQ CONTROLS: FULL CW (+6dB)
POS. PEAK AMPLITUDE: FULL CCW

STEP 3 Apply a 1kHz sinewave test signal to the LEFT INPUT of the Processor at a level which yields 10dB of peak limiting.

STEP 4 Monitor the output of the "left" channel (L+R) clipper buffer stage with the oscilloscope. The "bottom" of R47 (20k behind IC6, top center of card) is a convenient monitor point.

STEP 5 Adjust R38 (near the rear of the board) CCW until slight flattening of the waveform is observed, then set the control back CW to just eliminate visible clipping.

STEP 6 Replace the "left" limiter card in the chassis and extend the "right" limiter assembly (A/N 168101).

STEP 7 With the audio generator feeding the LEFT channel (as in STEP 3), repeat STEPS 4 and 5 for the "right" (L-R) limiter card.

STEP 8 Seal R38 on both limiter cards with a dot of Elmer's glue.

Phase Rotator Matching

STEP 1 Remove the "left" limiter board (A/N 168100) and disconnect the -00 jumper just behind the lower LED.

STEP 2 Preset the Processor as follows:

LEFT AND RIGHT CHANNEL LINE OUTPUT CONTROLS: FULL CCW
R20 (BEHIND THE LOWER LED), BOTH CHANNELS: FULL CW
PUT THE PROCESSOR IN PROOF.

STEP 3 Plug the "left" limiter card into the Processor via the extender.

STEP 4 Connect the AC voltmeter to the LEFT channel LINE OUTPUT. NOTE: This is a single-ended connection; use "+" and "GND."

STEP 5 Apply 100Hz from the audio generator to the LEFT INPUT at a level which yields a 0dBm reading on the voltmeter.

STEP 6 Adjust R20 on the "left" peak limiter card slowly CCW until the monitored output drops to -3dBm.

STEP 7 Re-install the "left" channel card (A/N 168100) and extend the "right" (A/N 168101).

STEP 8 Monitor the RIGHT channel LINE OUTPUT with the AC voltmeter ("+" and "GND"). That output should also measure approximately -3dBm.

STEP 9 Carefully adjust R20 on the "right" peak limiter card for a null in the output reading. When nulled, the residual signal should drop to at least -30dBm.

STEP 10 Seal R20 on both the "left" and "right" channel limiter cards with a dot of Elmer's glue.

STEP 11 Remove the 2k resistor and re-install the jumper across the -00- terminals on the "left" limiter board.

VIII APPENDIX

Parts Lists

Schematic Diagrams

Warranty

SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
		STEREO A.G.C. ASSEMBLY (A/N 165200)
A1,2	1335	CMOS Quad Analog Gate; RCA CD4066BE
C1,2,7,11, 12,17	0827	Capacitor, Dipped Mica, CM05; 300pF
C3,4,13,14	1073	" Tantalum; 10uF, 25V
C5,15	0822	" Dipped Mica, CM06; 1000pF
C6,9,10,16, 19,20	0824	" " " " 1500pF
C8,18	0814	" " " CM05; 220pF
C21	1054	" Tantalum; 4.7uF, 25V
C22	0865	" Mylar; .047uF, 100V
C23	0818	" Dipped Mica, CM06; 470pF
C24	1065	" Tantalum; .22uF, 35V
C25	1067	" " 1uF, 35V
C26,27	0835	" Dipped Mica, CM06; 2000pF
C28-31	1053	" Tantalum; 2.2uF, 25V
CR1-5	1100	Diode, Silicon Signal; 1N4151 or equivalent
I1	2012	Miniature Lamp; Type 327 or 387
IC1-3	1375	Integrated Circuit; National LF353N
IC4,5	1313	" " Raytheon RC4558NB
Q1-4	1204	Transistor, NPN; National PN3567
Q5	1205	" PNP; " PN3645
R11,31	0508	Potentiometer, Multi-turn, 2k; Spectrol 43P202T050
R60	0556	" Single Turn, 1k; Beckman Helipot 91AR-1k
		NOTE: All fixed resistors are 1/4-watt, 5% carbon film; value in ohms per schematic notation.
S1,2	1826	Switch, 2-Pole, 3-Position; Continental Wirt G-128S/G20-18
S3	1829	" DPDT; Continental Wirt GMB126/G-20-76

SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
BANDPASS COMPRESSOR ASSEMBLY (A/N 194800)		
Capacitors		Polarized capacitors are 25-volt electrolytic, radial leads, value per schematic. Other capacitors are 5% polyester, value per schematic; "minibox" type with 0.2" lead spacing; WIMA MKS-2 or FKC-2 series or equivalent.
CR1-10	1100	Diode, Silicon Signal; 1N4151 or equivalent
IC1-7	1375	Integrated Circuit, LF353N (Mfgr. open)
IC8,9	1335	Integrated Circuit, CD4046BE (Mfgr. open)
Resistors		All Fixed resistors are 1/4-watt, 5% carbon film; value per schematic.
FM PEAK LIMITER ASSEMBLY (A/N 194500)		
Capacitors		Polarized capacitors are 25-volt electrolytic, radial leads, value per schematic. Other capacitors are 5% polyester, value per schematic; "minibox" type with 0.2" lead spacing; WIMA MKS-2 or FKC-2 series or equivalent.
CR1,2	1127	Diode, Schottky; Hewlett-Packard 1N5711
CR3-6	1100	Diode, Silicon Signal; 1N4151 or equivalent
IC1,2,4,7,8	1375	Integrated Circuit, LF353N (Mfgr. open)
IC3	1313	Integrated Circuit, RC4558NB (Mfgr. open)
IC5,6	1335	Integrated circuit, CD4066BE (Mfgr. open)

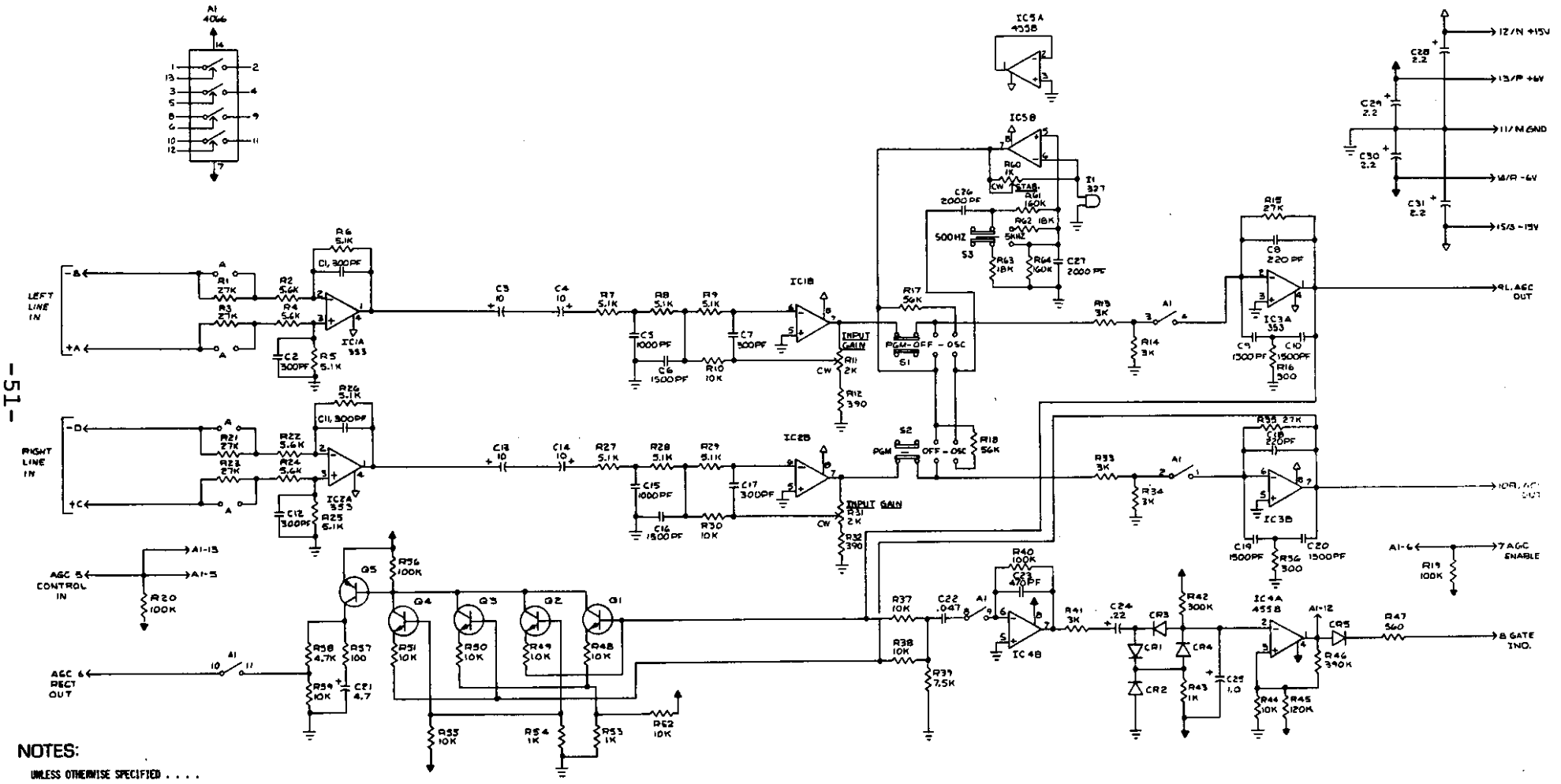
SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
L1	1403	Inductor, 1mHy; Delevan 2500-28
R1	0513	Potentiometer, multi-turn, 50k; Beckman 43P503T050
R23	0556	Potentiometer, single-turn, 1k; Beckman 91AR-1K
Resistors		All Fixed resistors are 1/4-watt, 5% carbon film; value per schematic.
AM PEAK LIMITER ASSEMBLY (A/N 168100 / 01)		
A1,2	1335	CMOS Quad Analog Gate; RCA CD4066BE
C1	0818	Capacitor, Dipped Mica, CM06; 470pF
C2,4	0822	" " " 1000pF
C3	0814	" " " CM05; 220pF
C5	1065	" Tantalum;.22uF, 35V
C6	0828	" Dipped Mica, CM06; 750pF
C7,8,9	0892	" Polystyrene/Polypropylene; .0047uF, 160V
C10	0824	" Dipped Mica, CM06; 1500pF
C11	0834	" " " 1200pF
C12	0811	" " " CM05; 120pF
C13	0862	" Mylar; .01uF, 100V
C14	0915	" Electroyltic; 47uF, 25V
C15,16,20-23	1053	" Tantalum; 2.2uF, 25V
C17,18	0867	" Mylar; .1uF, 100V
C19	1067	" Tantalum; 1uF, 35V
C24	1071	" Electrolytic; 22uF, 25V
CR1,2,5-7	1100	Diode, Silicon Signal; 1N4151 or equivalent
CR3,4	1127	" Schottky; Hewlett-Packard 5082-2800
I1,2	2014	Light-Emitting Diode, Red; Litronix RL4850

SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
IC1,3,7,9	1314	Integrated Circuit; Signetics NE5535N
IC2,4,6	1375	" " National LF353N
IC5,8	1313	" " Raytheon RC4558NB
L1	1403	Inductor, 1mH; Delevan 2500-28
R20	0559	Potentiometer, Single Turn, 10k; Beckman Helipot 91AR-10k
R38	0556	" " " 1k; " " 91AR-1k
R24	0510	" Multi-turn, 10k; Spectrol 43P103T050
R50	0513	" " 50k; " 43P503T050
		NOTE: All fixed resistors are 1/4-watt, 5% carbon film; value in ohms per schematic notation.
LOG FUNCTION CONVERTER ASSEMBLY (A/N 164600)		
C1,6,10	1054	Capacitor, Tantalum; 4.7uF, 25V
C2,3,11-13	1053	" " 2.2uF, 25V
C4,5,7,8	1067	" " 1uF, 35V
C9	1071	" " 22uF, 20V
CR1-34,36,37	1100	Diode, Silcon Signal; 1N4151 or equivalent
CR35	1106	" Germanium Signal; 1N34 or equivalent
IC1-4	1313	Integrated Circuit; Raytheon RC4558NB
IC5	1314	" " Signetices NE5535N
Q1-5,12-14, 18-21	1204	Transistor, NPN; National PN3567
Q6-10,15,16	1205	" PNP; National PN3645
Q11,17	1235	" FET; Siliconix J108
		NOTE: All fixed resistors are 1/4-watt, 5% carbon film; value in ohms per schematic notation.

SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
PWM ASSEMBLY (A/N 164400)		
C1-4,9-13	1053	Capacitor, Tantalum; 2.2uF, 25V
C5	0801	" Dipped Mica, CM05; 10pF
C6	0818	" " " CM06; 470pF
C7	0822	" " " " 1000pF
C8	0810	" " " CM05; 100pF
CR1-10	1100	Diode, Silicon Signal; 1N4151 or equivalent
IC1-8	1317	Integrated Circuit; National LM311N
IC9,10	1354	" " RCA CA3100E
IC11	1373	" " National LM317T
Q1-8	1204	Transistor, NPN; National PN3567
Q9	1235	" FET; Siliconix J108
R20	0558	Potentiometer, Single Turn, 5k; Beckman Helipot 91AR-5k
		NOTE: All fixed resistors are 1/4-watt, 5% carbon film; value in ohms per schematic notation.
STATIC PROGRAMMING ASSEMBLY (A/N 164200)		
C1-3	1053	Capacitor, Tantalum; 2.2uF, 25V
CR1	1105	Diode, Zener, 12V; 1N5242 or equivalent
CR2-40	1100	" Silicon Signal; 1N4151 or equivalent
IC1-6	1332	Integrated Circuit, RCA CD4051BE
IC7	1357	" " RCA CD4042BE
R1-4,10-13, 19-22, 28-31	0559	Potentiometer, Single Turn, 10k; Beckman Helipot 91AR-10k
		NOTE: All fixed resistors are 1/4-watt, 5% carbon film; value in ohms per schematic notation.
S1-4	1853	Switch, 8-station DIP; Eeco 24000-8GB
S5	1854	" 10-position BCD; Eeco 2301-02G

SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
	ACTIVE PROGRAMMING ASSEMBLY [COMPUTER INTERFACE] (A/N 169200)	
	DECODER BOARD (SCHEMATIC 171400)	
C1	1053	Capacitor, Tantalum; 2.2uF, 25V
C2	1073	" " 10uF, 20V
C3	0850	" Mylar; .001uF, 100V
C4	0864	" " .01uF, 100V
CR1	1125	Diode, Rectifier; 1N4005 or equivalent
CR2,3	1100	" Silicon Signal; 1N4151 or equivalent
IC1,2		Integrated Circuit; National 74LS09N
IC3	1339	" " RCA CD4072BE
IC4	1343	" " RCA CD4093BE
IC5		" " General Instrument AY3-1015D
	CONTROLLER BOARD (SCHEMATIC 171100)	
C1,2	1053	Capacitor, Tantalum; 2.2uF, 25V
C3,4	0801	" Dipped Mica, CM05; 10pF
CR1-9	1107	Diode, Zener, 6.8V; 1N5235 or equivalent
IC1		Integrated Circuit; National LM78L12CZ
IC2-7	1332	" " RCA CD4051BE
IC8-15		" " National MM74C175N / DC40175BCN
IC16		" " RCA CD4060BE
		NOTE: All resistors are 1/4-watt, 5% carbon film; value in ohms per schematic notation.
Y1		Crystal, HC33; 2.4576MHz

SCHEMATIC DESIGNATION	INOVONICS PART NO.	GENERIC PART DESCRIPTION AND / OR MANUFACTURER'S ID & PART NO.
DISPLAY ASSEMBLY	(A/N 165400)	
C1-4	1053	Capacitor, Tantalum; 2.2uF, 25V
I1-85	2019	Light-Emitting Diode, Red; Stanley SPR5731
IC1-8	1376	Integrated Circuit; National LM3914N
IC9	1332	" " RCA CD4051BE
CHASSIS ASSEMBLY		
C1,2	1064	Capacitor, Disc Ceramic; .005uF, 1000V
C3	0902	" Electrolytic; 1000uF, 35V
C4	0910	" " 470uF, 50V
C5-8	1053	" Tantalum; 2.2uF, 25V
CR1-8	1125	Diode, Rectifier; 1N4005 or equivalent
IC1,3	1373	Integrated Circuit; National LM317T
IC2,4	1374	" " " LM337T

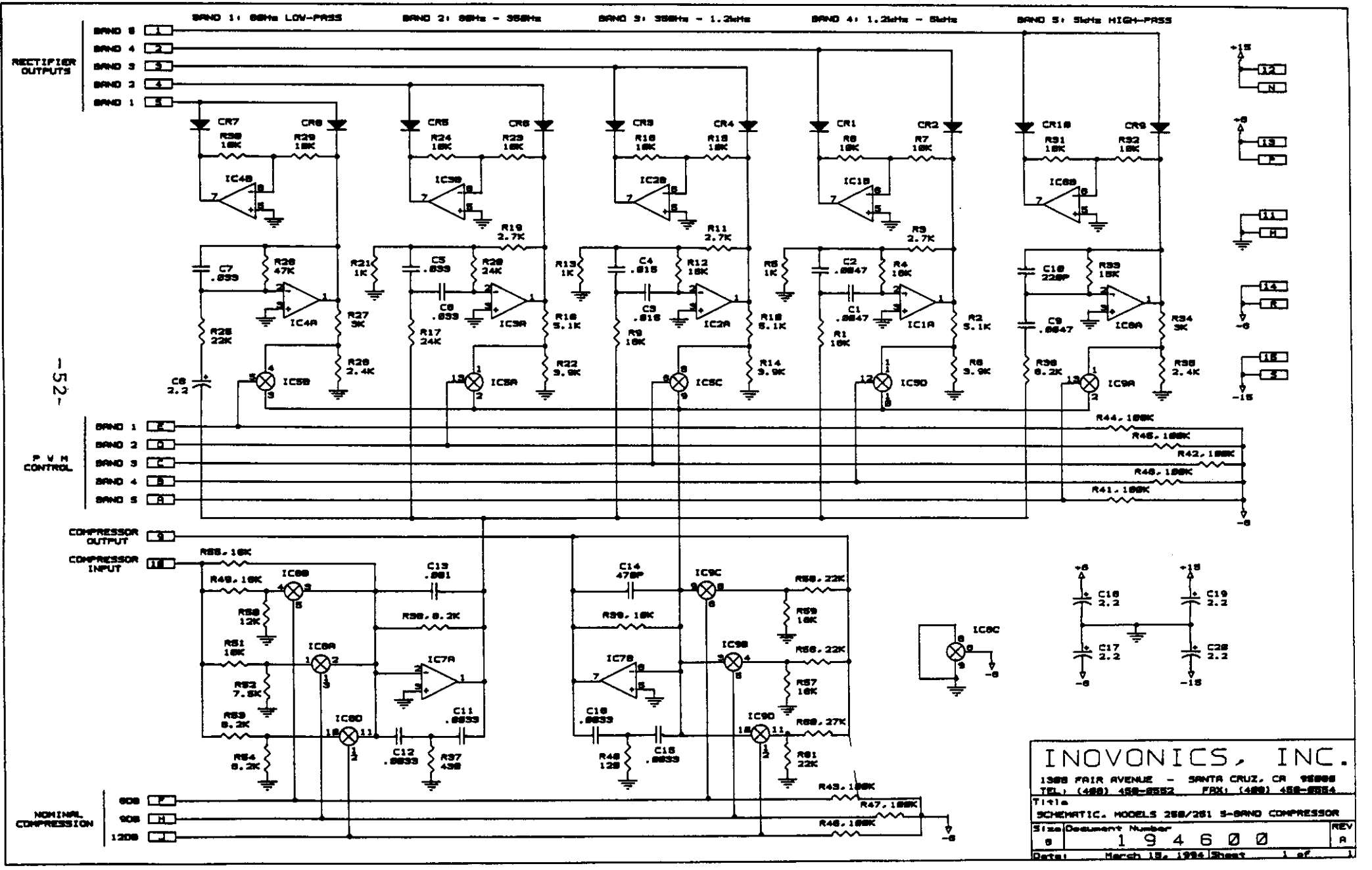


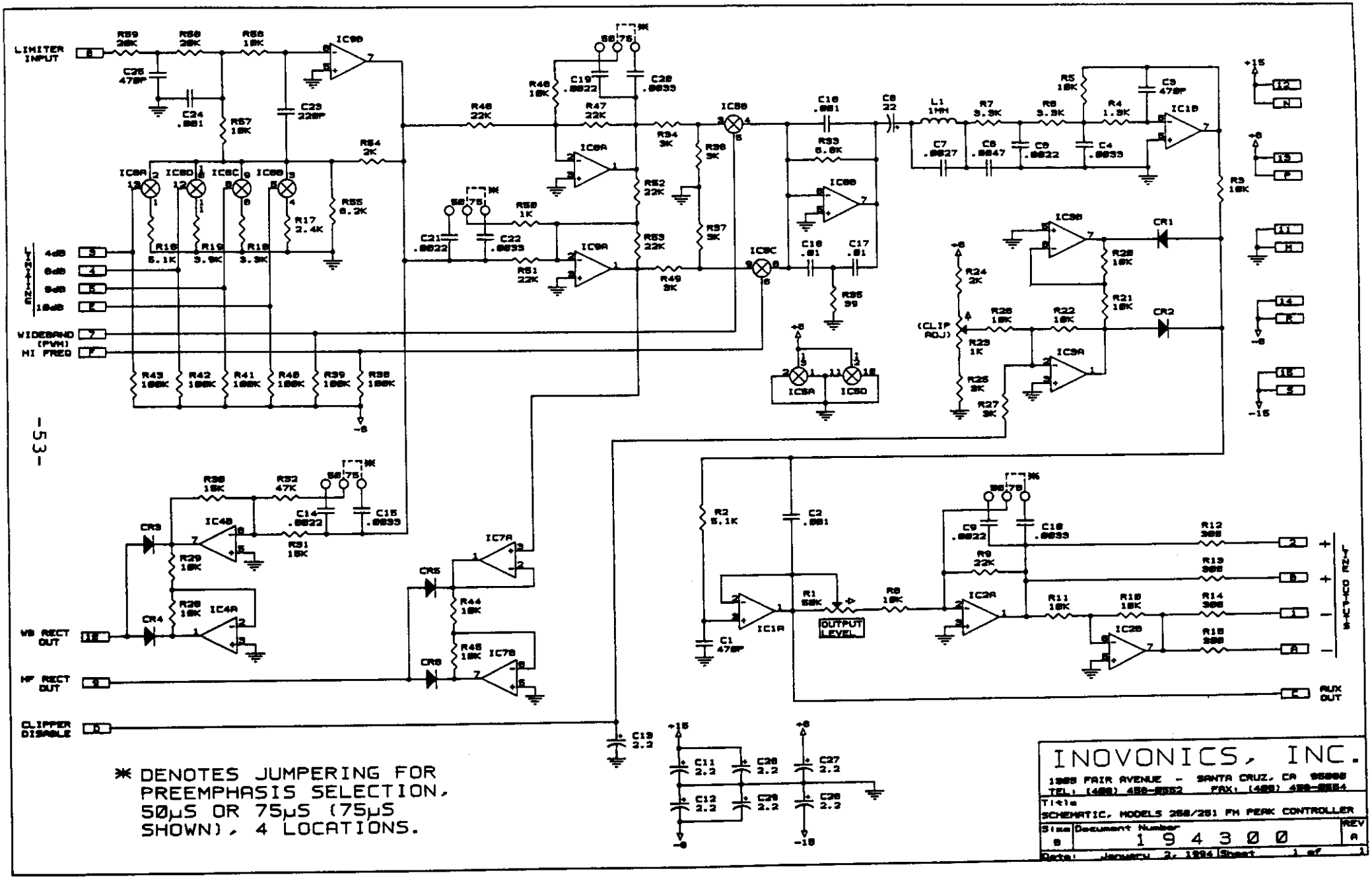
NOTES:

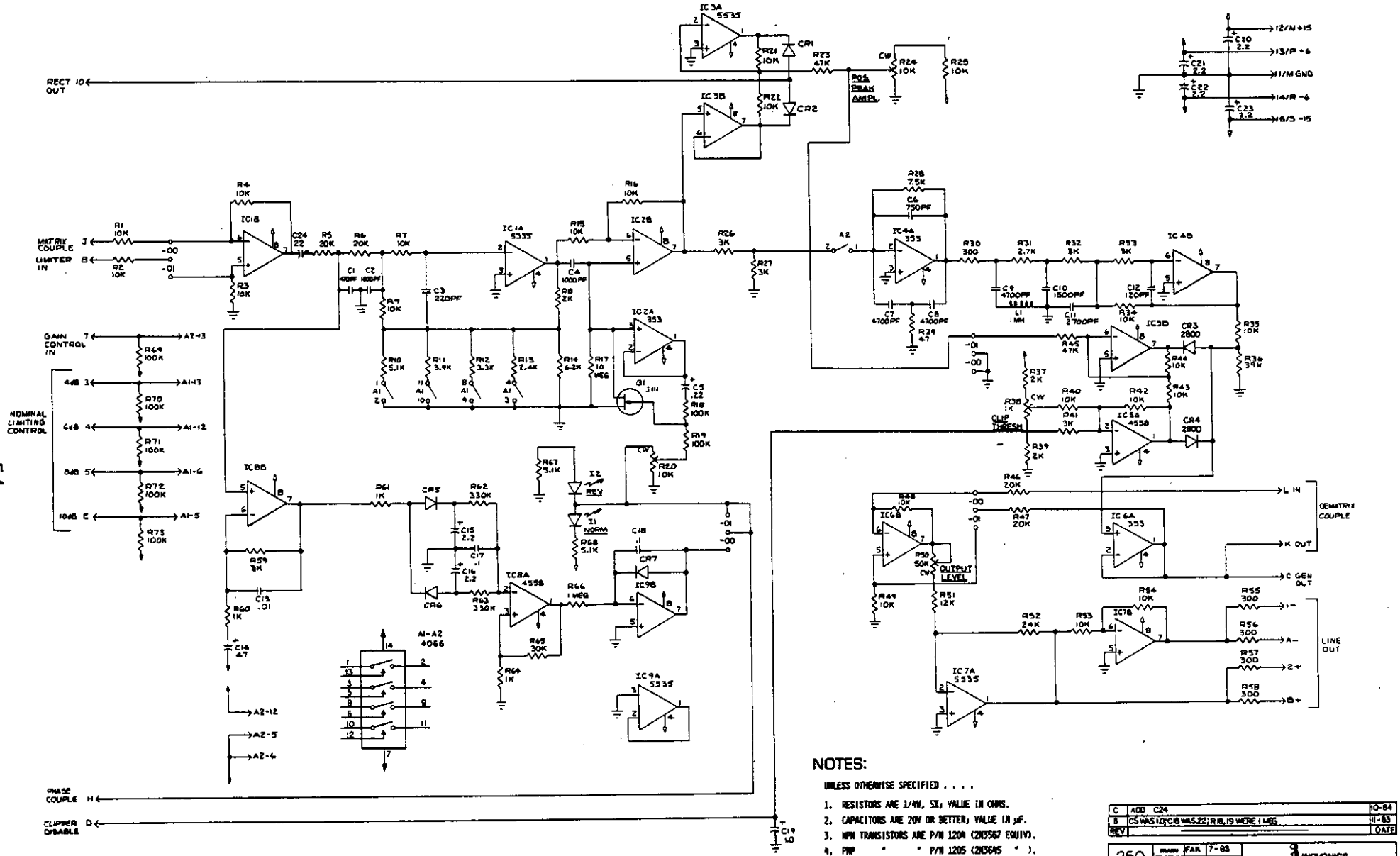
UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. NPN TRANSISTORS ARE P/N 1200 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

250	DRAWN	FAR	11-82	INOVONICS
	CHECKED	JBW	1-24-83	
	APPROVED			TITLE: SCHEMATIC, STEREO A.G.C.
	MATERIAL / FINISH	—		SHEET 1 of 1 — DWG NO 170500 — ISSUE A


BAND 1: 60Hz LOW-PASS
BAND 2: 60Hz - 350Hz
BAND 3: 350Hz - 1.2kHz
BAND 4: 1.2kHz - 5kHz
BAND 5: 5kHz HIGH-PASS
RECTIFIER OUTPUTS
BAND 5
BAND 4
BAND 3
BAND 2
BAND 1
PWM CONTROL
COMPRESSOR OUTPUT
COMPRESSOR INPUT
NOMINAL COMPRESSION
60B
90B
120B
INOVONICS, INC.
1308 FAIR AVENUE - SANTA CRUZ, CA 95060
TEL: (408) 458-0552 FAX: (408) 458-0554
Title
SCHEMATIC, MODELS 258/261 5-BAND COMPRESSOR
Size B
Document Number 194600
REV A
Date: March 15, 1994 Sheet 1 of 1


LIMITER INPUT
4dB
6dB
9dB
18dB
WIDEBAND (PWM) HI FREQ
WB RECT OUT
HF RECT OUT
CLIPPER DISABLE
(CLIP ADJ)
OUTPUT LEVEL
AUX OUT
* DENOTES JUMPERING FOR PREEMPHASIS SELECTION, 50µS OR 75µS (75µS SHOWN), 4 LOCATIONS.
INOVONICS, INC.
1305 FAIR AVENUE - SANTA CRUZ, CA 95060
TEL: (408) 458-0552 FAX: (408) 458-0554
Title
SCHEMATIC, MODELS 258/251 FM PEAK CONTROLLER
Size B
Document Number 194300
REV A
Date: January 2, 1994 Sheet 1 of 1



NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

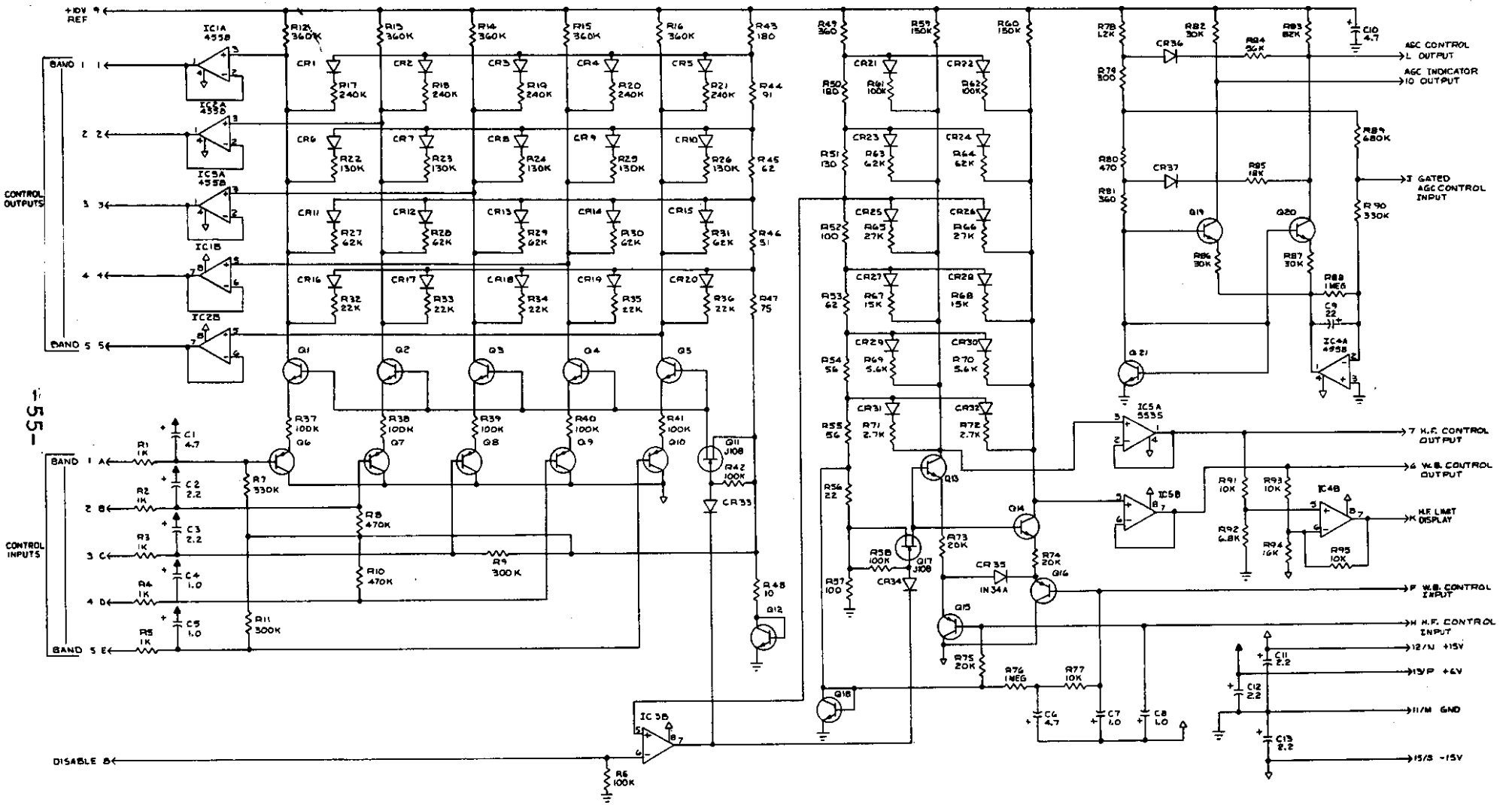
REV		DATE
C	ADD C24	10-84
B	C5 WAS 10; C16 WAS .22; R18,19 WERE 1 MEG	11-83

250 — DRAWN FAR 7-83; CHECKED JBW 8-4-83; APPROVED

INDYMICS

SCHEMATIC, A M PEAK LIMITER

PAGE 1 of 1 — DWG NO 170300 — REV C



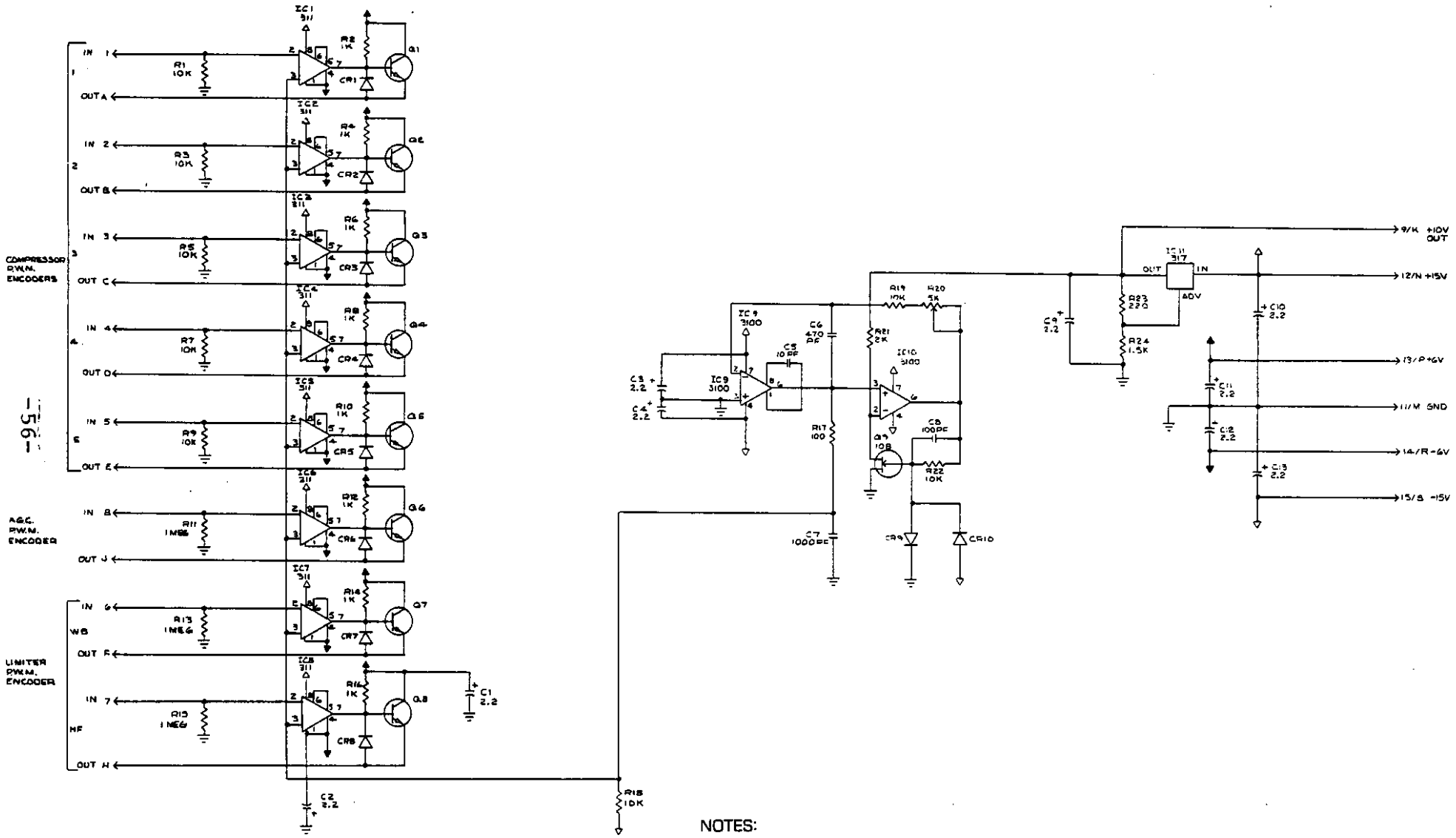
1551

NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN µF.
3. NPN TRANSISTORS ARE P/N 1201 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (NPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

250	DRAWN FAK 11-82	INOVONICS	
	CHECKED JBW 1-24-83	TITLE SCHEMATIC, LOG FUNCTION BOARD	
	APPROVED	PAGE 1 of 1	DWG NO 170100 REV A
TOLERANCES	MATERIAL / FINISH		

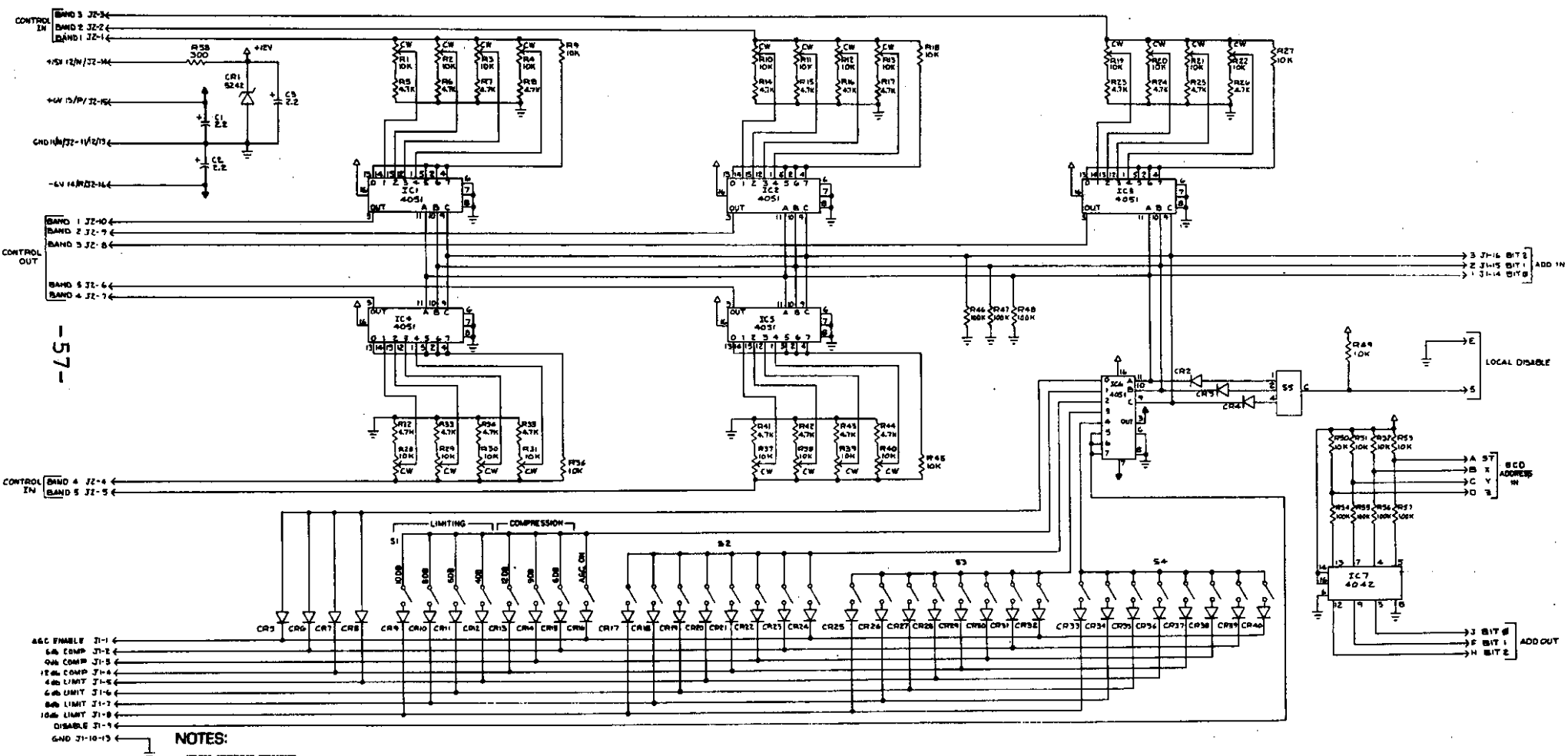


NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

250	DRAWN	FAK	11-82	INOVONICS
	CHECKED	JBW	1-25-83	
	APPROVED			TITLE: SCHEMATIC, PWM. BOARD
	MATERIAL / FINISH			SIZE: A — DRAWING NO: 170000 — REV: A

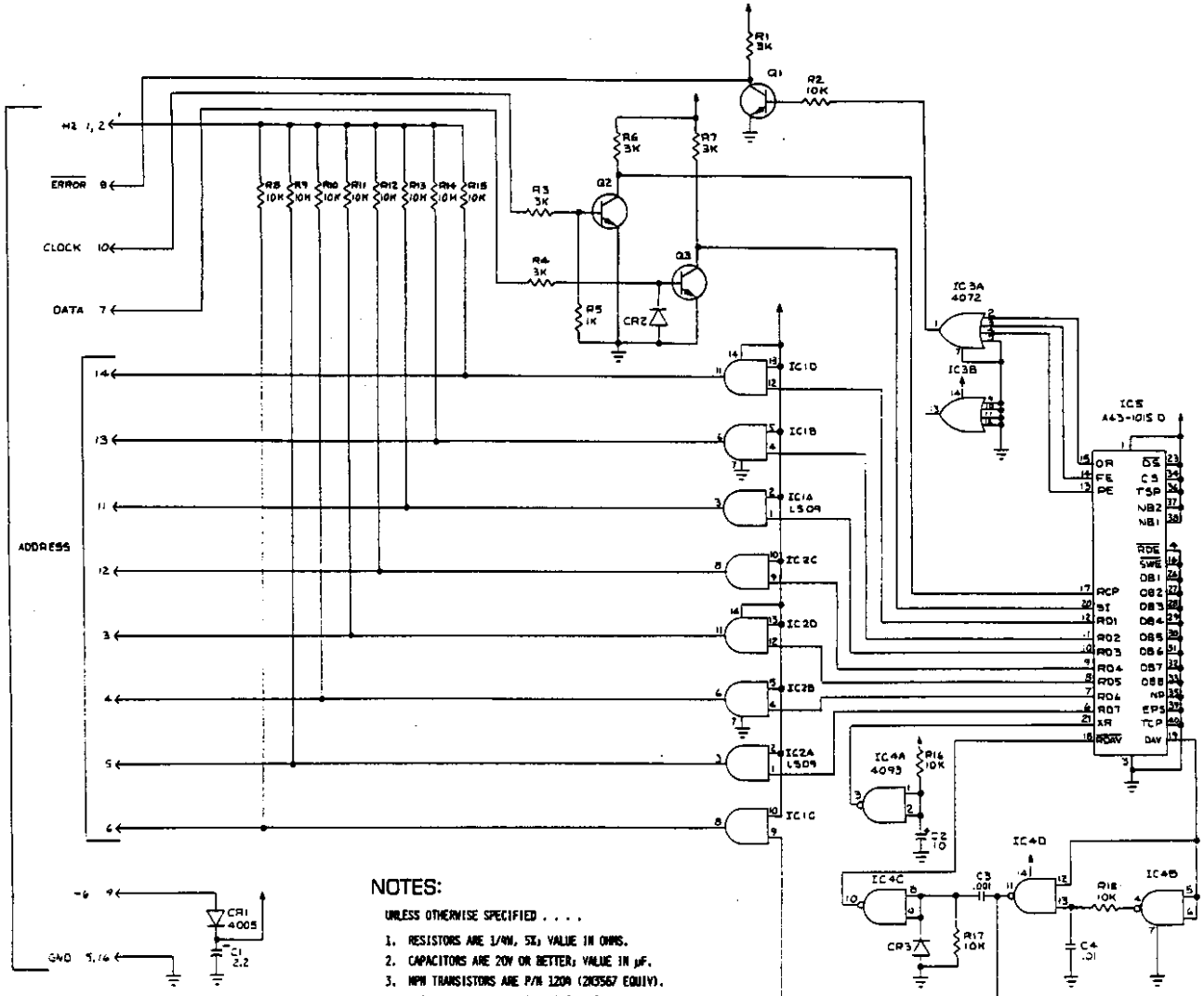


NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%, VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. NPN TRANSISTORS ARE P/N 1201 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (NPT 111 ").
6. DIODES ARE P/N 1108 (1N4151 EQUIV).

250	FAK 11-82	SCHEMATIC, STATIC PROGRAMMING BOARD	
	JBW 1-24-83	SIZE B	DWG NO 169800



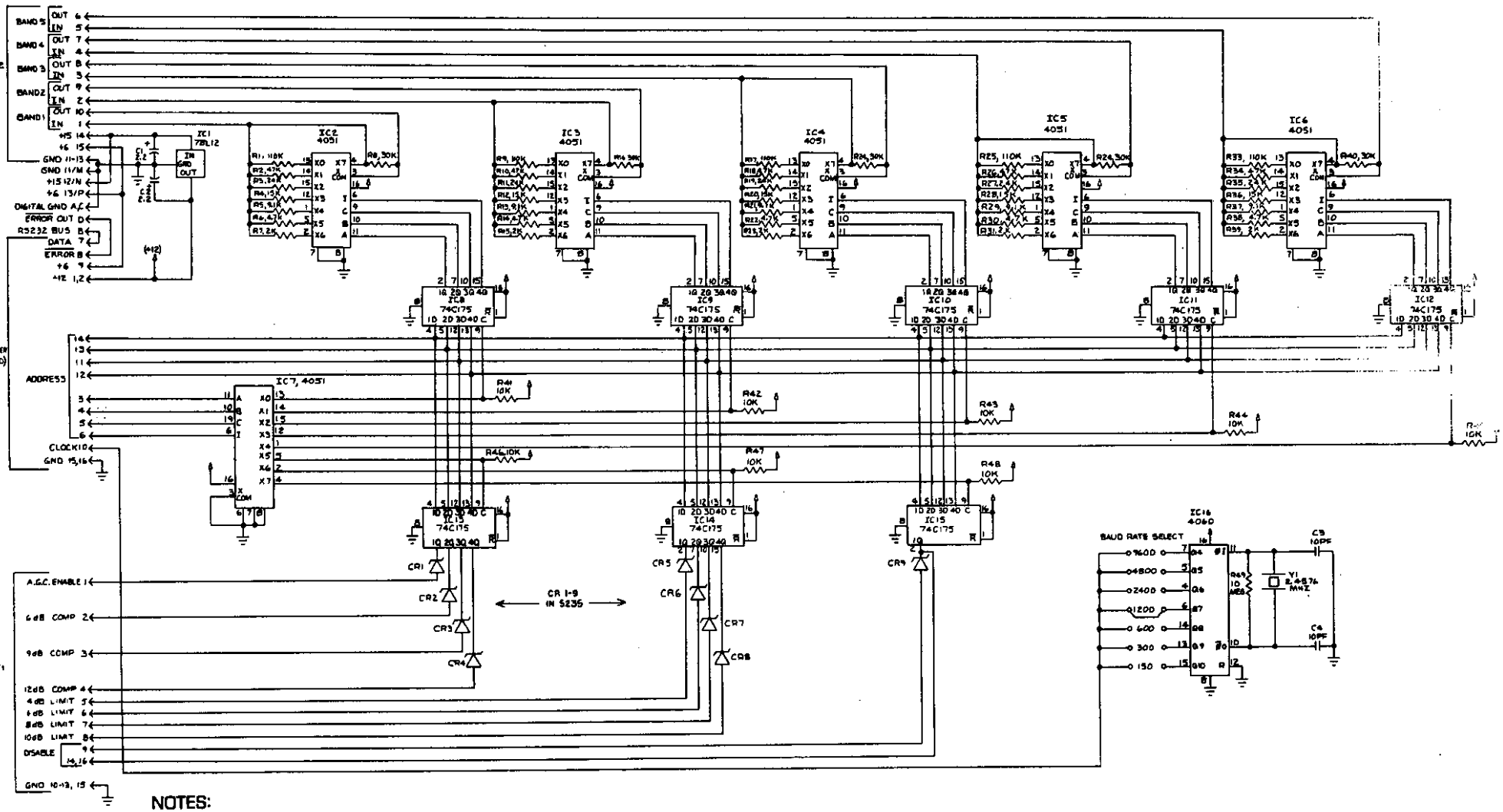
J1
(TO J2 OF CONTROLLER BOARD)

NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

250	DRAWN FAK 7-83	INOVONICS	
	CHECKED JBW 8-5-83		
	APPROVED	TITLE SCHEMATIC, COMPUTER INTERFACE-DECODER BRD.	
TOLERANCES	MATERIAL / FINISH —	PAGE 1 OF 1	DWG NO 171400
			ISSUE A



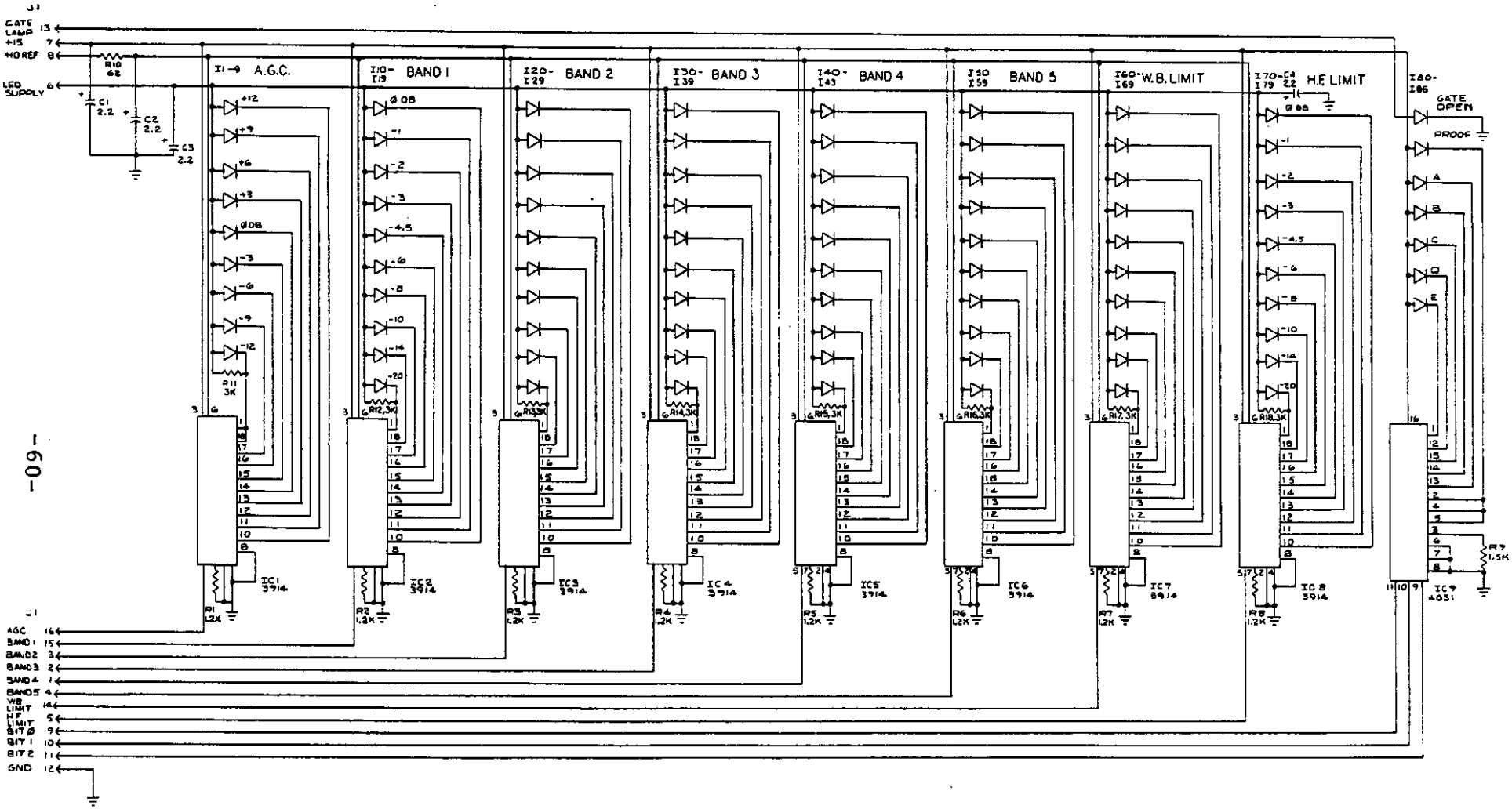
-59-

NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (NPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

250	DRAWN	FAK	8-83	INOVONICS
	CHECKED	JBW	9-7-83	SCHEMATIC, COMPUTER INTERFACE-CNTRLR. BRD.
	APPROVED			
	MATERIAL / FINISH	—		171100 A



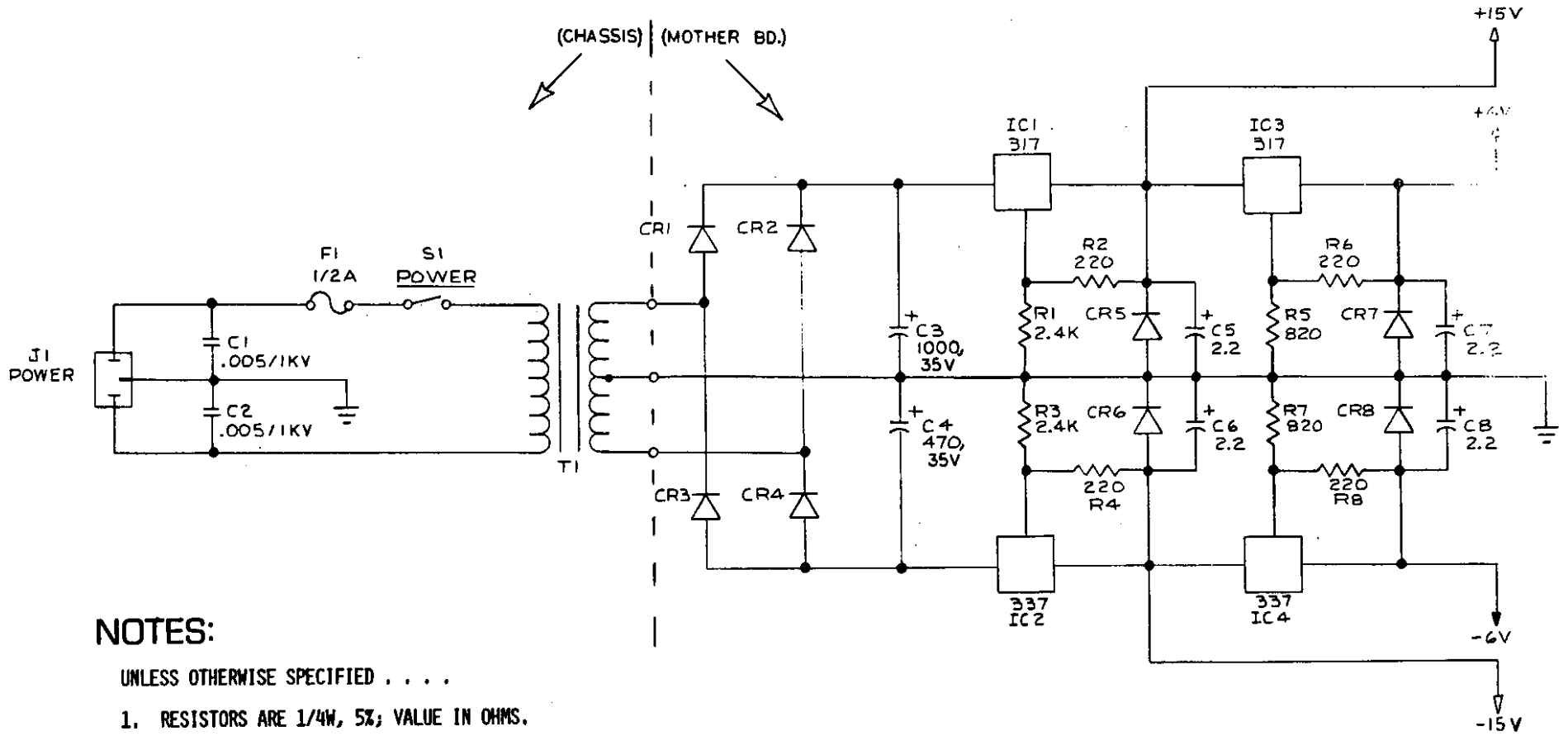
-60-

NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. NPN TRANSISTORS ARE P/N 1204 (2N3567 EQUIV).
4. PNP " " P/N 1205 (2N3645 ").
5. FET " " P/N 1211 (MPF 111 ").
6. DIODES ARE P/N 1100 (1N4151 EQUIV).

250	DRAWN FAK 11-82	INOVONICS	
	CHECKED JSW 1-24-83		
	APPROVED	TITLE SCHEMATIC, DISPLAY BOARD	
	MATERIAL —	PAGE 1 OF 1	DWG NO 170600 A

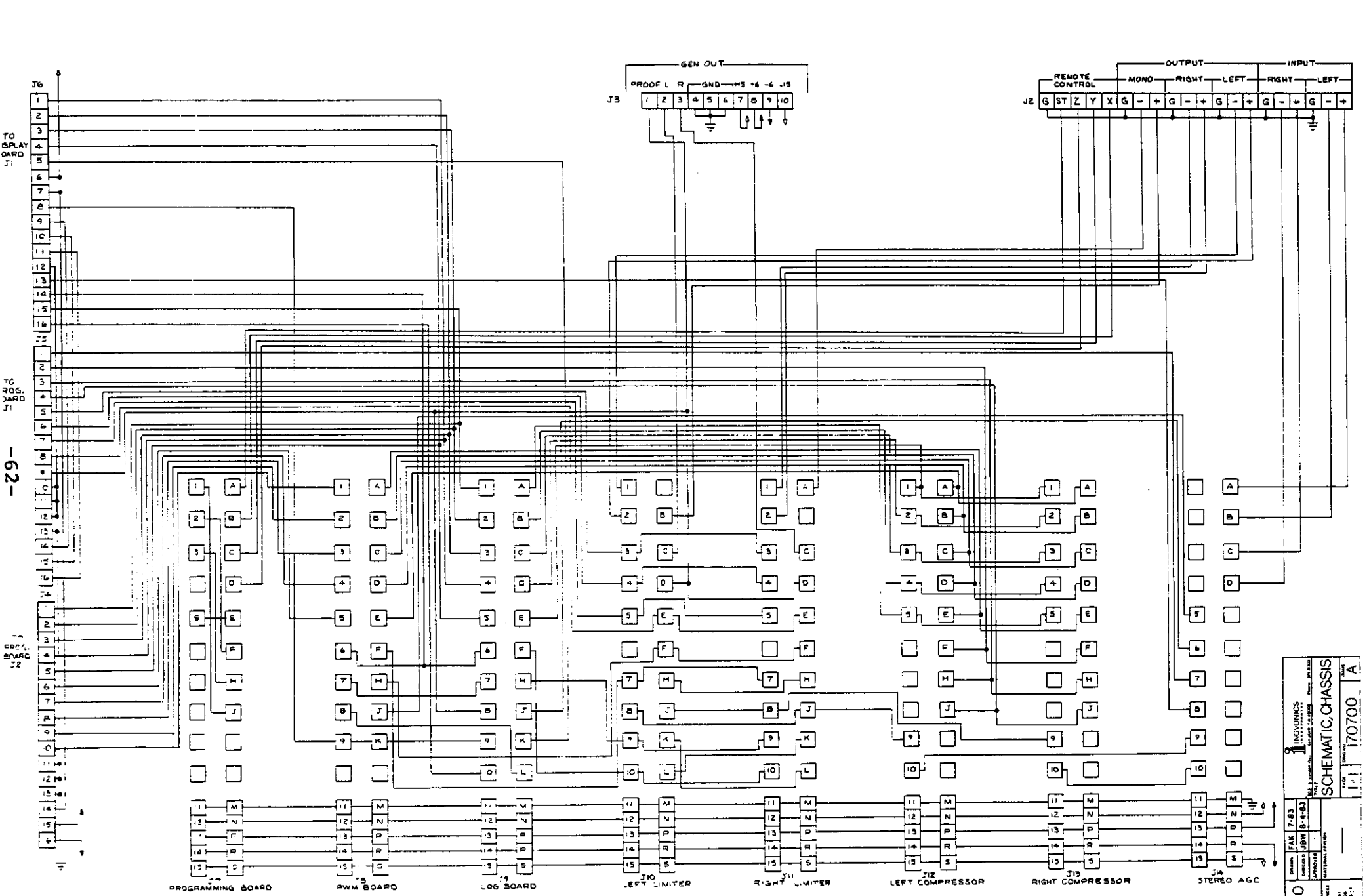


NOTES:

UNLESS OTHERWISE SPECIFIED . . . .

1. RESISTORS ARE 1/4W, 5%; VALUE IN OHMS.
2. CAPACITORS ARE 20V OR BETTER; VALUE IN μF.
3. DIODES ARE P/N 1125 (IN4005 EQUIV)

250	DRAWN	FAK	7-83	INOVONICS INCORPORATED 503-B Vandell Way Campbell, CA 95008 Phone 374-8300
	CHECKED	JBW	8-5-83	
	APPROVED			TITLE: SCHEMATIC, POWER SUPPLY
TOLERANCES: 2PL ± .01, 3PL ± .005, ANGLES ± 1°	MATERIAL / FINISH: —			PAGE 1 OF 1 · DWG NO 170800 · ISSUE A



INDUSTRIES
SCHEMATIC, CHASSIS
170700
A
250

INOVONICS WARRANTY

Inovonics, Inc. products are warranted to be free from defects in material and workmanship. Any discrepancies noted within 90 days of the date of purchase will be repaired free of charge. Additionally, parts for repairs required between 90 days and one year from the date of purchase will be supplied free of charge, with installation billed at normal rates. It will be the responsibility of the purchaser to return equipment for warranty service to the dealer from whom it was originally purchased unless prior arrangement is made with the dealer to inspect or repair at the user's location.

This warranty is subject to the following conditions:

1. Warranty card supplied with the equipment must be completed and returned to the factory within 10 days of purchase.

2. Warranty is void if unauthorized attempts at repair or modification have been made, or if serial identification has been defaced, removed, or altered.

3. Warranty does not apply to damage caused by misuse, abuse, or accident.

4. Warranty valid only to original purchaser.

INOVONICS
INCORPORATED